

# THE **pcb** **design** MAGAZINE

December 2014

**HDI PWB Reliability**  
by Paul Reid p.28

ALSO:

**PCBs for Medical Applications—  
A Designer's Perspective**  
by Kenneth MacCallum p.38

AN  I-CONNECT  PUBLICATION

## HIGH DENSITY INTERCONNECTS

# HDI LAYER STACKUPS FOR LARGE, DENSE PCBs

by Charles Pfeil and Happy Holden, page 10

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## ***This Issue: HIGH DENSITY INTERCONNECTS***

### **FEATURED CONTENT**

More and more designers are moving into the realm of HDI, which frees up real estate and allows more components to be placed on the board. This month, our expert HDI contributors explain the finer points of designing fine lines and blind and buried vias.

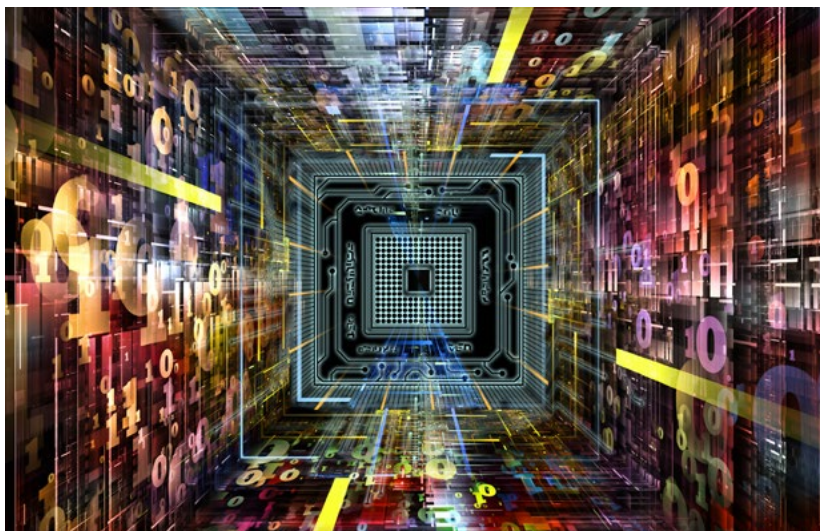
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*by Charles Pfeil and Happy Holden*



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*by Paul Reid*







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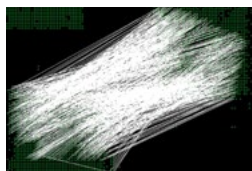


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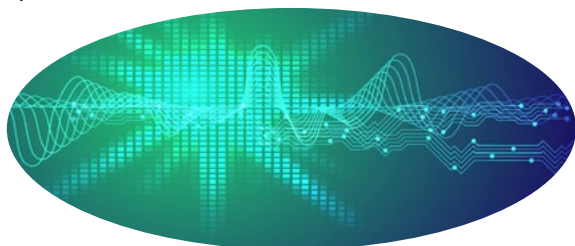
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# IPC's Holiday Gift to Industry: Dieter 2.0

by Daniel J. Smith  
RAYTHEON

We have all seen business leadership change as time passes. Some leaders have chosen to retire early, like Bill Gates of Microsoft, but some people have left us through death, such as Steve Jobs of Apple.

Both men were the icons, the “face” of their company’s ups and downs. There was a succession plan in place to have a new leader take command, to continue the company’s spirit and quality, but with a new vision. Each of their successors has also had his ups and downs, too, but they are the new face to those that buy and support those products.

And then there was IPC’s Dieter Bergman. Dieter was a caring, giving man to all he met. It did not matter if you agreed with him on every detail of a technology standard or topic;

you were in the presence of a man who gave his all for a company and an industry he truly loved.

Dieter was the “face of IPC,” and it is to his empty pedestal that we all cast our gaze. This assembly of the curious is looking for the next icon of IPC’s technology direction. That icon will be known simply as “Dieter 2.0.”

I know that Dieter’s assignments have been spread around within IPC to various people, staffers who may or may not have his SMEs (subject matter expert’s) knowledge or passion. These assignments must be re-codified and reassigned back to the new person, Dieter 2.0. This will allow everyone to sigh with relief. We need a new standard-bearer for the thousands of volunteers who give up months of man-work-







Figure 1: Dieter Bergman left a void in the industry. Who will be Dieter 2.0?

hours every year for creating IPC standards for Paul Eisler's industry.

So, just as a child assembles his Christmas list, I have created a similar wish list of who I believe IPC needs to seek out to be their next IPC representative:

1) A visionary: The person needs to examine the previous vision of where IPC was going, but also have a new vision of what both IPC and the industry requires in order to be productive and a continuing presence and force.

2) A selfless team player: This person should be one who listens and builds consensus for the good of the entire PCB industry, and not be driven by a personal or hidden agenda.

3) A technologist: This person should have acquired a majority of their cognitive knowledge from spending time in the trenches of this industry. There is no amount of reading that will prepare this person for what is truly needed to understand the chemistry of fabrication and assembly knowledge, as well as why the IPC standards have been authored in the manner they have for all of these years.

4) A historian: Dieter 2.0 must understand the history of where IPC has been. This will prove critical to formulating our collective direction going forward. It will be important to avoid "rat holes" of previous initiatives that have produced little or negative progress for IPC and the industry.

5) A listener: The majority of IPC is made

up of participants from all aspects of the PCB design process. Every participant has a voice and an idea that needs to be shared and heard. This person needs to let these ideas come out and help shape the overall direction of our future.

6) A consensus builder: Dieter 2.0 must sort out all of this information from the participants, and use their powers of communication to ensure that a collective direction forward on a subject has the support of the majority—for the good of the majority.

It would be great if there was a "recipe" for creating a clone of Dieter. But, as we all know, it is more important to be your own true leader than be just like your predecessor.

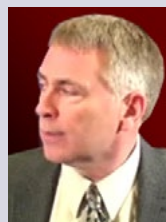
Dale Sevrey, one of my many managers over the years, offered me sound personal advice regarding death: "Everyone grieves differently."

In reflecting on Dale's words, I cannot rush IPC to hurry this grieving process. I respect everyone who works within (and for) this organization. I can only offer one request:

If the grieving process has completed, it would be a great present to the industry if you would select a person to be our future "presence."

If Dieter 2.0 could first be announced, and then formally introduced at IPC APEX EXPO 2015, I am sure there would be a surge in attendance just to meet and greet this new technologist and continue their allegiance to volunteering for IPC.

I wish all of you a happy and safe holiday season with time to reflect on the joys and sorrows of this past year, and to offer thanks in prayer in anticipation of a great future for all in the coming year. **PCBDESIGN**



Daniel J. Smith is a principal technologist for Raytheon Missile Systems. He has taught multiple aspects of the PCB design process internationally, and he has authored several PCB-related patents, articles, and standards over the past 30+ years. To contact Smith, [click here](#).

# HDI LAYER STACKUPS FOR LARGE, DENSE PCBs

**by Charles Pfeil**

MENTOR GRAPHICS

**Happy Holden**

CONSULTANT

This article is intended to help those who are doing large, dense PCBs with multiple high pin-count BGAs, and finding standard laminate stackups inadequate to meet their cost and performance goals. Maybe your laminate board has too many layers, or the feature sizes prevent effective breakout and routing of the BGAs. HDI stackups are a viable alternative and can provide lower cost with higher performance if designed properly.

Hopefully from this article you will be able to determine which stackup methodology is best for your designs and why the alternatives may not be appropriate. To find out which stackups are recommended, you can skip to the end of the document. However, if you want to understand the reasons why these stackups are recommended and the impact of choosing one of the alternatives, then it would be best to read the whole article.

Defining the appropriate stackup should be considered as one of the most important aspects of initial design work. Since there are so many

variables involved with stackups, this article will focus on stackups that will enable effective design of boards with multiple large, dense BGAs. Typically this includes boards for the networking, computer, server, and emulation marketplace. It is assumed that even though handheld devices and consumer electronic products will likely have dense BGAs, it is unusual for them to have multiple instances exceeding 1500 pins and as such, do not present the kind of design challenges of concern herein.

## **Fabricators**

Stackups should be designed in conjunction with the fabrication vendor to minimize cost and meet signal integrity requirements. The board fabrication vendor ultimately builds a board that meets your requirements for cost, reliability, overall thickness, and impedance control. There may be additional requirements related to plating and specific materials. As a general rule, the vendor will adjust all the stackup variables as needed during their process to meet your goals. The most productive method is to agree with the vendor on a stackup prior to designing the board; then, the fabricator will need to make minimal adjustments to meet your goals.

Consider impedance control. Regardless of how carefully the stackup is defined with trace widths, material choices, dielectric and cop-



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VT-4B1	1.0W/m.K.	✓	✓	✓	✓
VT-4B3	3.0W/m.K.	✓	✓	✓	✓
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VT-4B7	6.5W/m.K.	✓	✓	✓	✓

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## HDI LAYER STACKUPS FOR LARGE, DENSE PCBs *continues*

per thicknesses, the fabrication process is not so exact. Each vendor has different equipment and methods. The lamination process shrinks the dielectrics and materials may be changed if not in stock or readily available. The tolerances in all areas add up and ultimately a reliable vendor has to make the right combination of adjustments in-process so that when measuring impedance on the test coupon, it fulfills your spec. Trace widths and material thicknesses may change a little, but if the measured impedance is within spec then it really doesn't matter what changes were made, as long as the other requirements are not fatally compromised, of course.

If the initial stackup is not defined properly, minor acceptable adjustments by the fabrication vendor will not be adequate to fulfill your overall requirements. A wise and experienced vendor will not accept the risk of making major changes to the design data.

### Dependencies

Unfortunately there are many dependencies, some of them circular when defining a stackup. The process of determining an effective stackup can be overwhelming. Forgive the next meandering and confusing paragraph, but this is a good example of the difficult process of deciding which variables need to be compromised or emphasized to reach your goals. It is necessary to reduce the layer count to keep costs down. On some of the largest PCBs, there are well over 10,000 nets, which require many layers for routing. To control crosstalk, you need to increase the spacing between traces which will likely necessitate even more layers. You may also want to run the diff pairs together through the via array under the BGA, which means the via must be small enough to not only allow the diff pair to run together, but also space the traces far enough apart to attain the desired coupling.

These traces also need to be the appropriate width in correlation to the thickness of the dielectrics and their material attributes to provide the desired impedance. But if you have too many layers, then the via needs to be bigger otherwise the aspect ratio of hole size to length becomes too great to drill with a good yield. If

you make the via hole smaller, you can enable more dense routing but may sacrifice manufacturing yields. If you make the via hole larger, you may have to split the diff pairs through the BGA fanout via array and negatively impact your signal integrity. If you have more layers because you have to split the diff pairs, you will need an even larger via. On top of that, all these factors may require you to develop special fanout patterns in the context of the stackup to support the manufacturing, signal integrity and routing goals. This paragraph touches just a few of the dependencies, yet even so, it describes a daunting task.

Where does one start, then? Later, you will see a number of example stackups with their advantages and disadvantages, plus a basic description of which via models and design rules work best. Some signal and power integrity concerns will also be addressed.

### Overview of Stackup Types

In the context of boards that have high pin-count BGAs, there are three stackup types of interest:

#### 1. Standard Lamination with Through Vias

##### Advantages

- Low cost (until layer count becomes too high).
- Simple via models.
- Simple dielectrics—primarily FR-4.
- Mature process. "Everybody does it."
- High reliability (until layer count becomes too high).

##### Disadvantages

- If layer count becomes too high.
- Fewer fabrication vendors can obtain good yields, costs skyrocket.
- Can delaminate under high temperatures required for ROHS lead-free soldering.
- Via has to be large, reducing route-ability, increasing layers.
- Difficult to implement for BGA pin-pitches below 1 mm.
- Through-hole vias capacitively couple to every plane layer, and signal losses increase with thickness.



- Long via stubs create impedance mismatches, reflections on single-ended nets.
- Large via pads often force diff pairs to be split under BGAs.

### **Recommendations**

There are a number of tipping points where standard lamination with through vias is not viable:

- Once the board is over 28 layers, it becomes difficult to manufacture with acceptable yields and therefore can become cost-prohibitive.
- If the board is over 28 layers, the dielectrics can be so thin that delamination can occur under the higher temperatures required for lead-free soldering.
- Generally when using a few BGAs with less than 1500 pins and a 1mm pin-pitch, the breakout and routing of these devices is feasible using through vias. However, if you have a large number of these on a single design, then the route density may force the layer count up high enough to limit the effectiveness of this stackup. If you have multiple BGAs with over 1500 pins and 0.8mm pin-pitch (or less) it is likely that through vias will make it very difficult to route these devices.
- When the thickness of the board, due to the number of layers, forces the via to be so large that it inhibits routability. Via length to hole diameter should be  $<10\times$ , or reliability will decline significantly. Pad diameter should be hole size plus 0.01". If the via pad is so large that it prevents diff pairs or multiple single-ended traces from being routed between the BGA via arrays, then more layers will be required to complete the routing. Vias can be shifted off the standard matrix under BGAs; however, with through vias, not much is gained.

## **2. Sequential Lamination with Blind and Buried Vias**

### **Advantages**

- Potentially shorter via stubs.
- Fairly simple via models.
- Generally smaller vias than required for through hole vias. Minimum size for mechanically drilled vias are the same as for standard laminate; however, blind and buried vias will likely have a smaller aspect ratio, enabling more use of minimum via hole size, which is 8<sup>th</sup>.
- Simple dielectrics, primarily FR-4.
- Effective use of blind & buried vias opens up routing channels, potential for fewer layers.

### **Disadvantages**

- Not a widely adopted process; more and more fabricators do HDI instead.
- Minimum size for drilled vias is 8<sup>th</sup>.
- Costs more than through hole laminated, yet minimum trace widths are still the same.
- Practical reliability limits the number of sequential laminations to 2 or 3.

### **Recommendations**

- Sequentially laminated boards have the same tipping points as standard laminates; however, since the via length to hole size aspect ratio will be less and pad sizes can be smaller, routability improves and it is less likely that the design would exceed 28 layers.
- Since the feature sizes for traces can vias are still the same as with standard laminate, designing with multiple large BGAs of  $< 1\text{ mm}$  is very difficult.

## **3. Buildup with Microvias (HDI)**

### **Advantages**

- Smaller feature sizes for vias and traces enable higher route density and fewer layers.
- Effective use of microvia patterns opens up routing channels, potential for fewer layers.
- Only practical way to design with multiple large BGAs having  $<0.8\text{ mm}$  pitch.
- Lowest cost for high density boards.
- Improved signal and power integrity, with appropriate stackup definition.

## HDI LAYER STACKUPS FOR LARGE, DENSE PCBS *continues*

- Materials do well in processes requiring RoHS.
- Newer materials are available at higher performance and lower costs. These new materials are not suitable for standard or sequential lamination.

### Disadvantages

- Complex via models—many variations and still evolving.
- Complex stackup definition.
- Effective design methods on large dense designs have not been widely understood and documentation is sparse.
- Predictive design guides and cost estimates not yet available.
- Although HDI fabrication is pervasive in the Pacific Rim and China, North America has been slow to adopt.

### Recommendations

- HDI is the best alternative to high layer-count and expensive standard laminate or sequentially laminated boards.
- The trend is for higher pin-count and finer pin pitch. The tipping point will occur when the >1500 pin BGAs use a .8 mm pitch. The only way to effectively breakout and route multiple instances of these devices on a single board will be with the smaller HDI feature sizes.
- HDI currently dominates the fabrication technology for handheld and consumer electronics. For large board designs, it will continue to grow.

### HDI Stackup Details

This section is provided as a reference describing the relevant HDI stackup information based on the IPC standard. In this section, Types I, II and III are described. Type III is the recommended configuration for large, dense boards with multiple high pin-count BGAs.

### IPC-2315 Design Guide for High Density Interconnects and Microvias

Published jointly with the Japan Printed Circuits Association, IPC/JPCA-2315 provides an easy-to-follow tutorial on the selection of HDI and microvia design rules and structures. It ad-

dresses various considerations when designing an HDI printed wiring board, including design examples and processes, selection of materials, general descriptions, and various microvia technologies. It offers designers and manufacturers one source for reliable design and manufacturability information for commonly produced HDI boards.

### HDI Type I

This construction uses both microvias and through vias in a structure consisting of a laminated core and a single micro via layer on at least one side.

#### Notes:

1. The number of layers in the laminated core varies and is limited by two factors
  - a. The through-via should have an aspect ratio (total length to hole size) less than 10x to maintain reasonable reliability.
  - b. If the FR-4 dielectrics become too thin, they will delaminate under higher temperatures required for lead-free soldering.

### Recommendations

- In the context of large dense boards with multiple high pin-count BGAs, this stackup will not be significantly better than laminate. The through via pads will need to be large. Using only a single microvia layer will limit the ability to benefit from the smaller via and trace feature sizes.

### HDI Type II

This construction uses microvias, buried vias, and may have through vias.

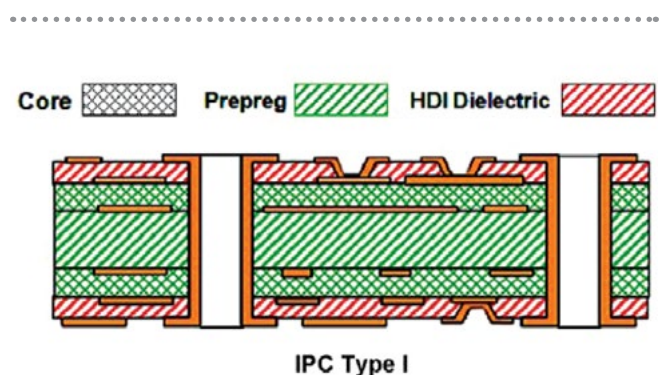


Figure 1: IPC Type I construction.



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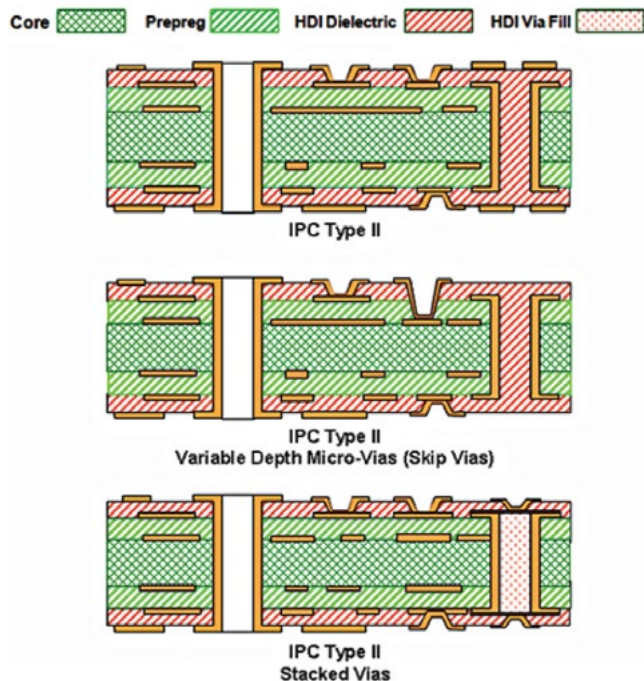


Figure 2: Various kinds of IPC Type II construction.

- There is a single microvia layer on at least one side.
- Via holes are drilled in a laminated core and become buried when the dielectric material is added for the microvias.
- Microvias are staggered from other microvias and may be stacked or staggered relative to the buried vias.

**Additional note:** See Type I note on limiting the number of laminated core layers, which applies to all variations of Type II through and buried vias.

### Recommendations

- In the context of large dense boards with multiple high pin-count BGAs, this stackup is better than Type I; however, it is not adequate for the more difficult designs. Using buried vias instead of the through vias is a significant advantage. Using only a single microvia layer will limit the ability to benefit from the smaller via and trace feature sizes.
- The single microvia layer also restricts

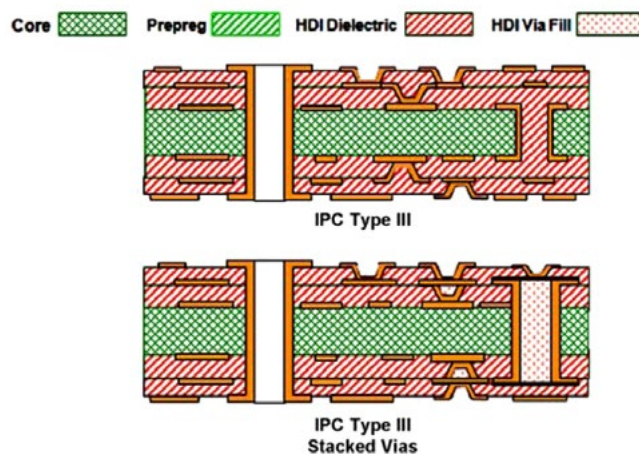


Figure 3: Example of IPC Type III construction.

the viability of using the outer layers for a GND plane. Having only one buildup layer for routing traces isn't nearly as effective as two.

### HDI Type III

This construction uses microvias, buried vias, and may have through vias.

- There are at least two microvia layers on at least one side.
- Via holes are drilled in a laminated core and become buried when the dielectric material is added for the microvias.
- Microvias may be staggered or stacked with buried vias.

**Additional note:** See Type I note on limiting the number of laminated core layers which applies to all variations of Type III through and buried vias.

### Recommendations

- HDI Type III is the best stackup configuration for large dense boards with multiple high pincount BGAs.
- With two microvia layers there is considerable routing area available using the smaller via and trace feature sizes.
- Using the outer layers for a GND plane is feasible because there are still enough microvia layers available for signal routing.



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## HDI LAYER STACKUPS FOR LARGE, DENSE PCBS *continues*

- Using stacked vias will allow for greater route density; however, the cost will be higher.

### HDI Type IV, V, VI

These additional HDI Types are defined in the IPC-2315 specification; however, they are not presented here simply because they are more expensive to fabricate and are probably not necessary for large, dense PCBs with BGA breakout and routing challenges.

### Via Models

HDI Type III accommodates numerous via models and spans. Ultimately the via model that suits your design best will be driven by finding the least expensive method that will still enable adequate route density within the constraints of signal integrity.

The graphic in Figure 4 presents some of the via models that may be used in HDI Type III.

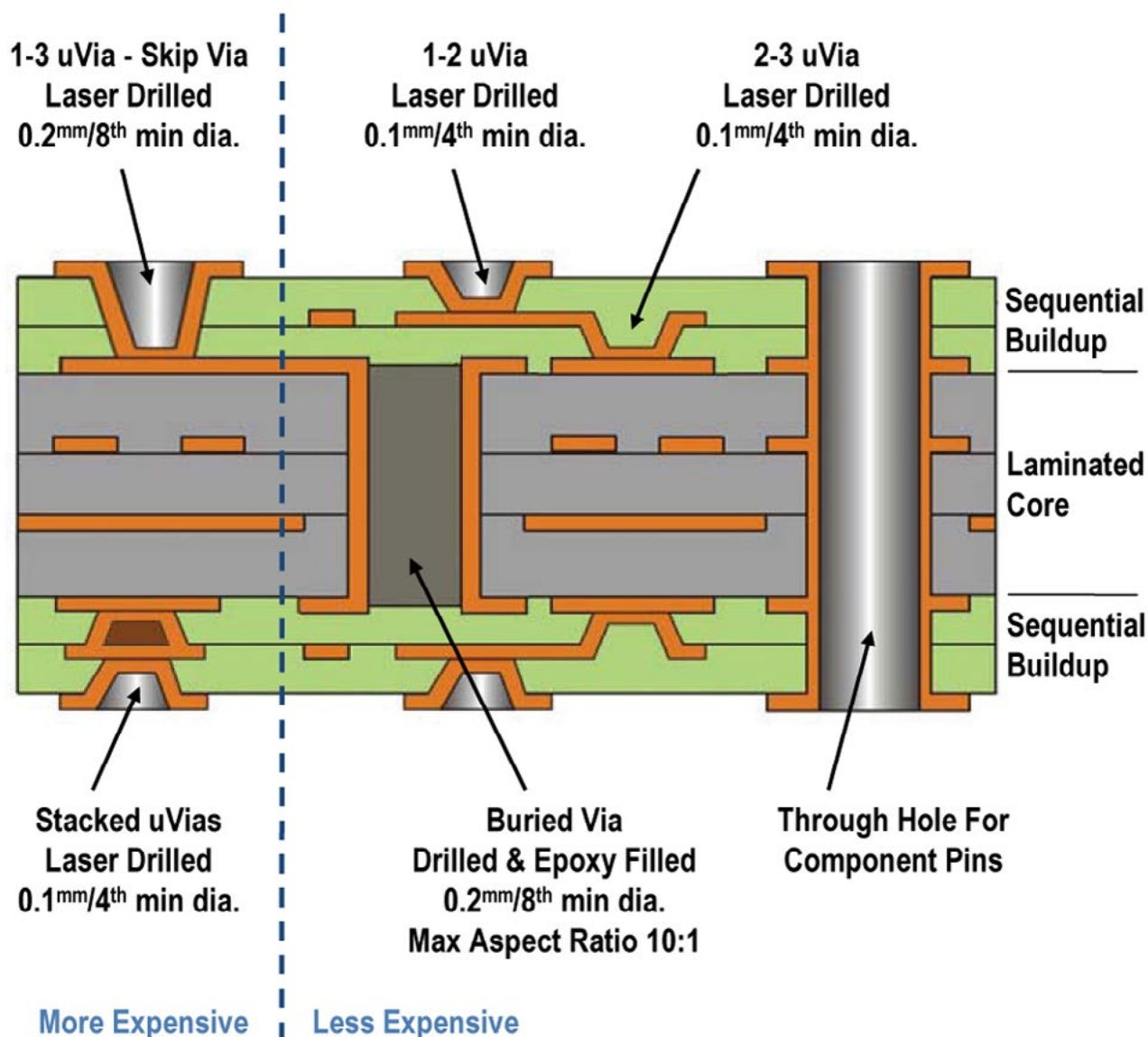


Figure 4: Examples of Type III construction.



- **Skip vias:** This via model is effective for transitioning layers (because it emulates the stacked via); however it is not as efficient as stacked vias for route space due to the fact that the minimum diameter is 8th.
- **Buried vias:** As a general rule, all unused pads on the buried vias should be removed. This will significantly reduce the crosstalk.
- **Microvia pad sizes:** Although the pad size will vary by fabricator, using a pad .15mm/6th larger than the hole is adequate.
- **Via aspect ratio:** Hole length to diameter for microvias is 5:1; for buried vias, 10:1.

### Alternative Via Spans

#### Stacking Microvias and Buried Vias

As seen in Figure 5, the microvias may be stacked upon each other, and/or with buried vias.

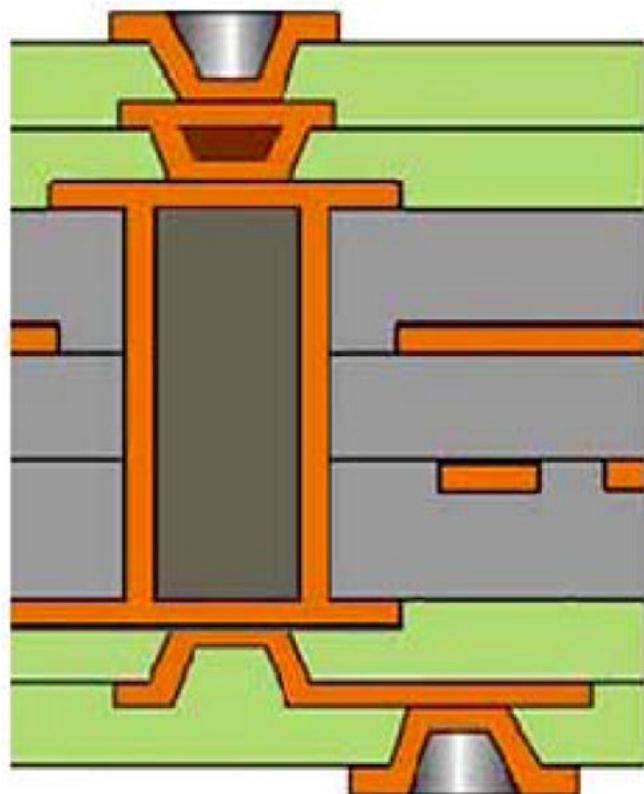


Figure 5: Examples of stacked microvias and buried vias.

#### Advantages

- Using stacked vias enables the most flexible and efficient via configuration for routing.

#### Disadvantages

- Stacking vias generally costs more due to the additional steps required to ensure a good connection between the vias.

#### Extending Buried Vias

As seen in Figure 6, you can extend the buried via into the first microvia layer.

#### Advantages

If you have power and ground nets that need to extend all the way through the board, using extended buried via uses less space.

#### Disadvantages

- Single-ended nets that use the extended blind via may suffer from additional via-stub effects; however, the additional stub length may be insignificant depending on the frequency.
- Depending on the fabricator, the cost of extending the buried-via may be slightly more than just having the buried-via in the laminated core.

#### Layer Count

The number of buildup and core layers required to route the board and fulfill the per-

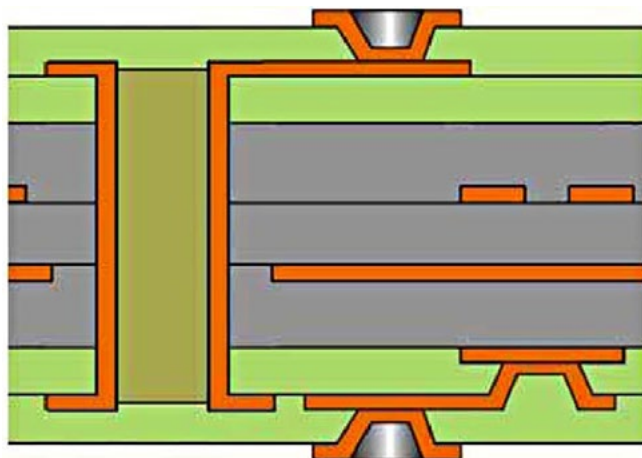


Figure 6: Example of a buried via extended into the first microvia layer.

## HDI LAYER STACKUPS FOR LARGE, DENSE PCBs *continues*

formance and signal integrity requirements will vary depending on the route density and manner in which you decide to manage the plane layer assignments. Determining the route density is a subject outside the scope of this article; however, as a general rule for large, dense boards, start with 8–10 signal layers and increase them as needed during the routing process.

Since the thickness of the laminated core will be limited by the aspect ratio of the buried via (10:1), work with your board fabricator to determine core and prepreg thicknesses. Doing this in conjunction with trying to minimize via pad size for routing will enable you to determine the high-end number of layers available in the laminated core.

### Design Rules

Throughout this paper, the minimum values for via hole sizes, pad sizes and the aspect ratios have been described. These minimums are used as a guide to enable high yields. Minimum trace widths and clearances are based upon the fabricator's capabilities; however, are more than likely to be set based on signal integrity requirements such as impedance control and minimizing crosstalk.

### Fanout Patterns

The method used for fanout of BGAs is a subject worthy of its own article, and can significantly contribute to the success or failure of the design. Here are some considerations:

#### Via location relative to BGA pad

- Adjacent (dog-bone)
- Partial via-in-pad
- Offset via-in-pad
- Via-in-pad

When using a combination of microvias and buried vias, each via span can have its own pattern within the BGA and as such can affect the routability of the device.

- Via-in-pad methods provide the greatest opportunity to increase route density.
- Shifting and aligning the vias is likely to improve routability.
- Using complementary patterns for the

microvias and buried vias can improve routability

- The goal should be to reduce the overall “effective” number of pins by the time you get to the laminated core, thus reducing the number of layers required to breakout and route the BGA.

### Recommended Stackup Criteria

A primary driver for going to HDI is to obtain sufficient route density to reduce layer count, thus lowering costs and improving reliability. Yet this must be done while maintaining power and signal integrity. Cost, density, power and signal integrity are the factors used in this paper to determine which stackups are recommended.

### HDI Cost

There are four drivers that determine the fabrication cost for HDI boards.

- **Materials:** Not only the type of material used but also the amount. So obviously a larger board will cost more than a smaller one.
- **Laminations:** The more lamination steps, the higher the cost. When buildup layers and via spans are mirrored about the core, then they can be done in the same lamination step. As you will see in the recommended stackups, the manner in which the via spans are defined affects the number of laminations.
- **Drills:** The more drill setups required, the higher the cost. A through-hole, buried via and a microvia each count as single drill setup. When buildup layers and via spans are mirrored about the core, then the microvia drilling on both sides is considered as one drill setup. The manner in which the via spans are defined affects the number of drill setups.
- **Plating:** Plating steps affects the cost, the more steps the higher the cost. These steps are used to plate the via wall and to ensure a reliable connection at the bottom of the drill. Using stacked vias and additional buildup layers generally increases the number of plating steps.



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## HDI LAYER STACKUPS FOR LARGE, DENSE PCBS *continues*

### Route Density

Microvias and smaller trace widths on build-up layers can significantly improve route density. Via-in-pad and stacking vias is also very good for improving route density. Using microvias and blind vias in certain patterns can open considerable space for routing on the laminate core layers. Ultimately, increasing route density will reduce your layer count and overall fabrication costs.

### Power Integrity

In the context of an HDI Type III stackup, location of the planes will impact your power distribution and integrity along with signal integrity. The appropriate location of planes is a much deeper and more complicated subject than can be addressed in this article; however, certain methodologies are recognized as effective and will be described at a high level here.

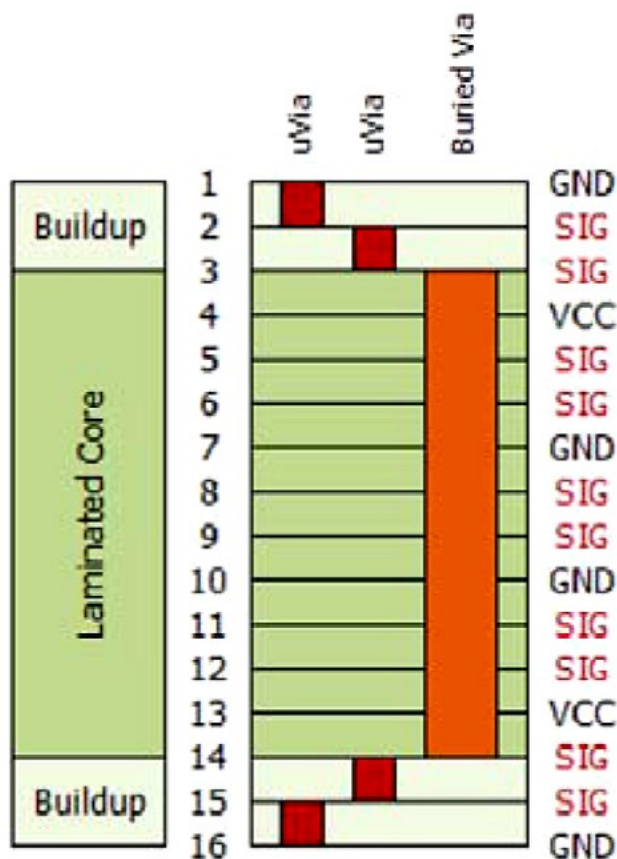


Figure 7: Typical stackup for GND assigned to outer layers.

In the stackups shown in Figures 7 and 8, the number of layers in the laminated core is variable; 16 layers is just convenient for the purpose of depicting plane layer assignments graphically.

**Outer Layer GND:** A stackup such as this is typical when GND is assigned to the outer layers.

### Advantages

- GND on the outer layers provide an excellent EMI shield.
- If you can place the bypass capacitors for the BGA on the same layer as the BGA, then you can minimize the number of vias used for GND underneath the BGA. This will open routing channels which may be critical for an extremely dense board. You may still want vias for some of the GND pins to improve the return paths.

### Disadvantages

- If you manage your return paths with an appropriate but not excessive number of GND vias under the BGA, then there really isn't a downside to using this method.
- Some may say that using the outer layers for GND will limit the number of buildup (smaller features) layers for routing signals. Although this is true, it is also important to consider that controlling the signal integrity of those nets will be more difficult and burying the first GND plane in the laminate structure will result in the routing on the microvia layers not having a good reference plane.

**Outer Layer GND & VCC:** A stackup such as this one is typical when GND and VCC are assigned to the outer layers.

**Note:** Using stacked vias would be good for this kind of stackup if it can be cost-justified.

### Advantages

Same advantages as listed for Outer Layer GND, plus these additional benefits:

- The capacitive coupling between the GND and VCC layers will be excellent,

minimizing the bypass capacitors needed for the BGA (assuming you use a relatively thin dielectric, less than .05 mm).

- This is also an opportunity to use embedded capacitors and pull-up resistors effectively. Considerable routing space would be opened on all signal layers.

### Disadvantages

If you manage your return paths with an appropriate but not excessive number of GND vias under the BGA, then there really isn't a downside to using this method.

**Split Planes:** Often large BGAs require multiple voltage supplies. You can use split planes or dedicated voltage layers for this power distribution. It would be best to add a couple of voltage supply layers in the center of the board, surrounded by GND planes to avoid having signal layers affected by crossing the splits or different voltages.

### Signal Integrity

This is a subject that has many dependencies, variables and thousands of articles. No attempt here to do anything but point out a few design methods related to large HDI stackups that will positively affect signal integrity.

- Remove unused pads on buried vias. This will reduce crosstalk significantly.
- Route the high-speed single-ended nets

on the buildup layers closest to the component. Stub effects are eliminated because buried vias are not used.

- Route diff pairs on the laminated core layers. The via stubs affect the diff pairs less than the single-ended nets and the crosstalk between the diff pair vias (if the unused pads are removed) is likely to be insignificant.
- A stripline configuration where pairs of signal layers are sandwiched between plane layers not only provides the best return paths but also reduce crosstalk. This supports the notion that using a GND plane on the outer layers is a good practice.

### Recommended HDI Type III Stackups

What are the best HDI stackups? It depends on your priorities. These stackups were analyzed for relative cost, route density, power integrity and signal integrity. The following three are rated A, B, and C, with the priority given to route density with good power and signal integrity.

#### Stackup A comments:

- This is a good average of the variables and a great stackup to start with if this is your first attempt at HDI.

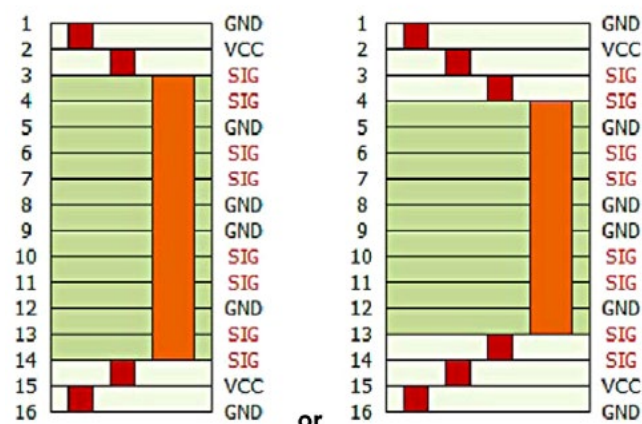


Figure 8: Typical stackup for GND and VCC assigned to outer layers.

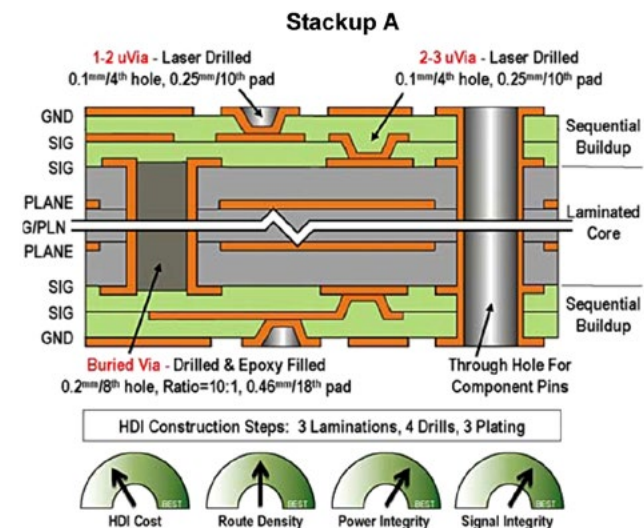


Figure 9: Stackup A, the best overall HDI stackup of the group.



## HDI LAYER STACKUPS FOR LARGE, DENSE PCBs *continues*

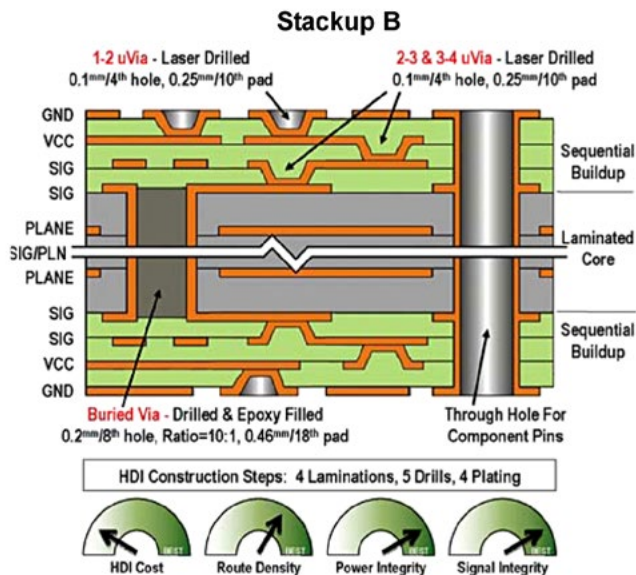


Figure 10: Stackup B, another good HDI stackup.

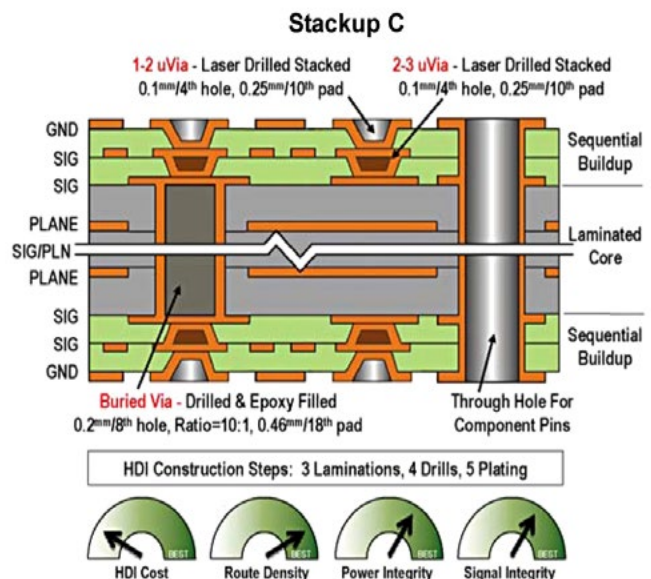


Figure 11: Stackup C, also a good HDI stackup.

- The via models are simple and it won't be difficult to find vendors who can fabricate it.
- The GND plane on the outer layers provides a high rating for power and signal integrity.

### **Stackup B comments:**

- The GND and VCC on the outer layers provide the best power and signal integrity.
- The additional buildup layer increases the cost (more laminations, drills and plating steps) but also improves the route density as opposed to losing an HDI routing layer due to the VCC plane.
- The via models are simple and it won't be difficult to find vendors who can fabricate it.

### **Stackup C comments:**

- The stacked vias enable the best route density but also increases the cost and may limit the number of vendors who can fabricate this stackup.
- The GND plane on the outer layers provides the high rating for power and signal integrity.

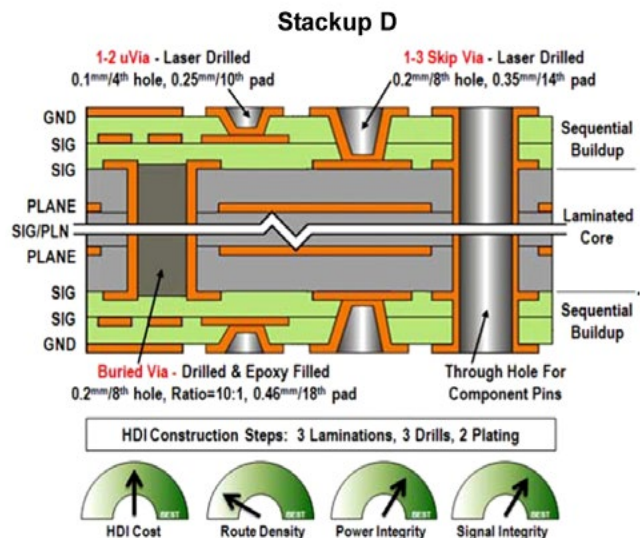


Figure 12: Stackup D, a secondary HDI stackup.

### **Secondary HDI Stackups**

These stackups are useful in their own way, depending on your priorities, but they are not as good overall as the Top 3.

### **Stackup D comments:**

- The GND plane on the outer layers provides a high rating for power and signal integrity.

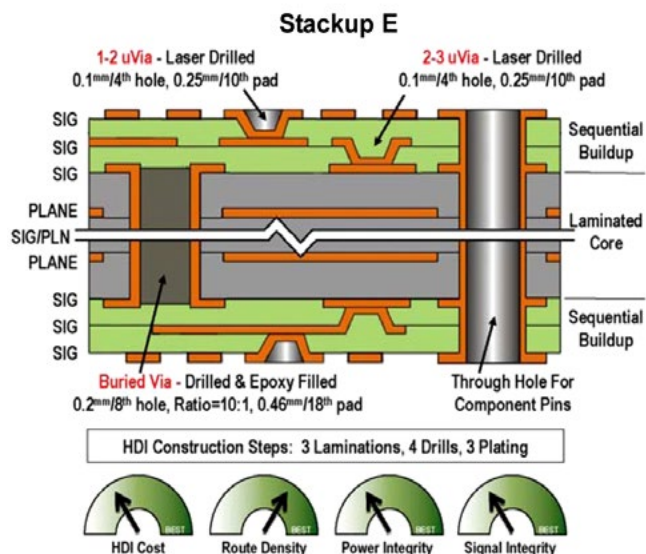


Figure 13: Stackup E, another secondary HDI stackup.

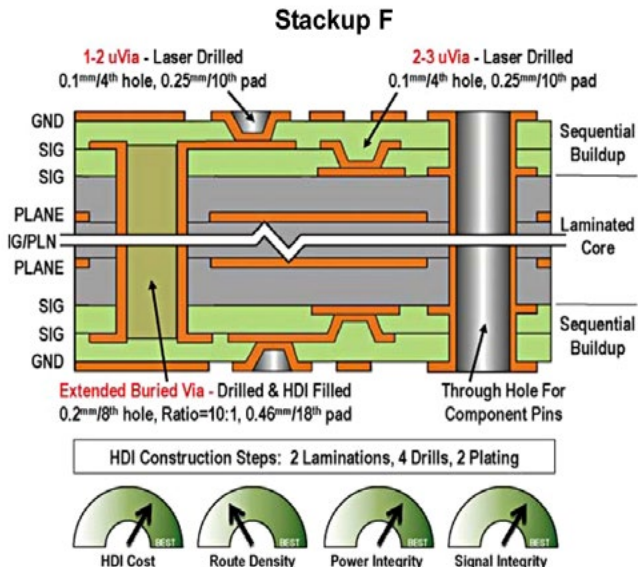


Figure 14: Stackup F, another secondary HDI stackup.

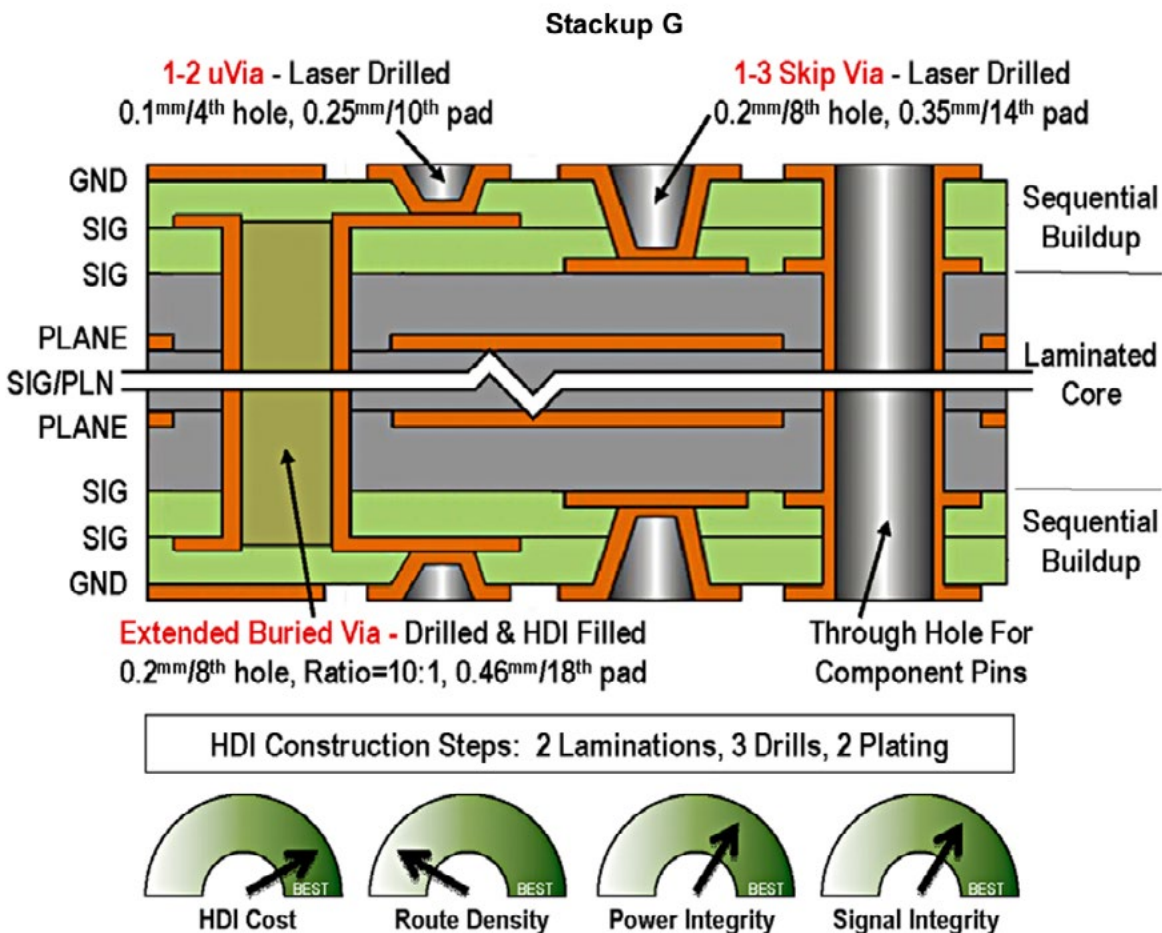


Figure 15: Stackup G, a final secondary HDI stackup.

## HDI LAYER STACKUPS FOR LARGE, DENSE PCBs *continues*

- The skip via reduces laminations and plating steps, which lowers cost; however, this contributes to a relatively low route density.

### **Stackup E comments:**

- The via models are simple and it won't be difficult to find vendors who can fabricate it.
- The lack of a GND plane on the outer layers reduces power and signal integrity; however, it does provide for improved route density assuming routing would be done on the outer layers.

### **Stackup F comments:**

- The GND plane on the outer layers provides the high rating for power and signal integrity.
- The extended buried via reduces lamination and plating steps, which lowers cost; however, it also reduces route density.

### **Stackup G comments:**

- The GND plane on the outer layers provides the high rating for power and signal integrity.
- The extended buried via and the skip via reduces the lamination and plating

steps which lowers cost; however it also reduces route density. **PCBDESIGN**



Charles Pfeil is an engineering director in the Systems Design Division at Mentor Graphics. He was the original product architect for Xpedition PCB and an inventor of XtremePCB. Pfeil has been in the PCB industry over 40 years as a designer, owner of a service bureau, and has also worked in marketing and engineering management at Racal-Redac, ASI, Cadence, PADS, and VeriBest. To contact him, [click here](#).



Happy Holden has been working with printed circuits in various capacities since 1970. He retired from Hewlett-Packard after nearly 29 years, and was senior PCB technologist for Mentor Graphics' System Design Division. Happy also served as a senior technologist with Foxconn and Gentex before retiring, finally, in 2013. He's currently working with Clyde Coombs on the 7<sup>th</sup> edition of the PCB Handbook, due out in mid-2015. To contact him, [click here](#).

## Noise Floor for Ultrasensitive Electronics Identified

A team of engineers and scientists has identified a source of electronic noise that could affect the functioning of instruments operating at very low temperature. The findings, detailed in the journal *Nature Materials*, could have implications for the future design of transistors and other electronic components.

The electronic noise the team identified is related to the temperature of the electrons in a given device, which in turn is governed by heat transfer due to packets of vibrational energy, called phonons, that are present in all crystals.



"A phonon is similar to a photon, which is a discrete packet of light," says Austin Minnich, an assistant professor of mechanical engineering and applied physics in Caltech's Division of Engineering and Applied Science and corresponding author of the new paper.

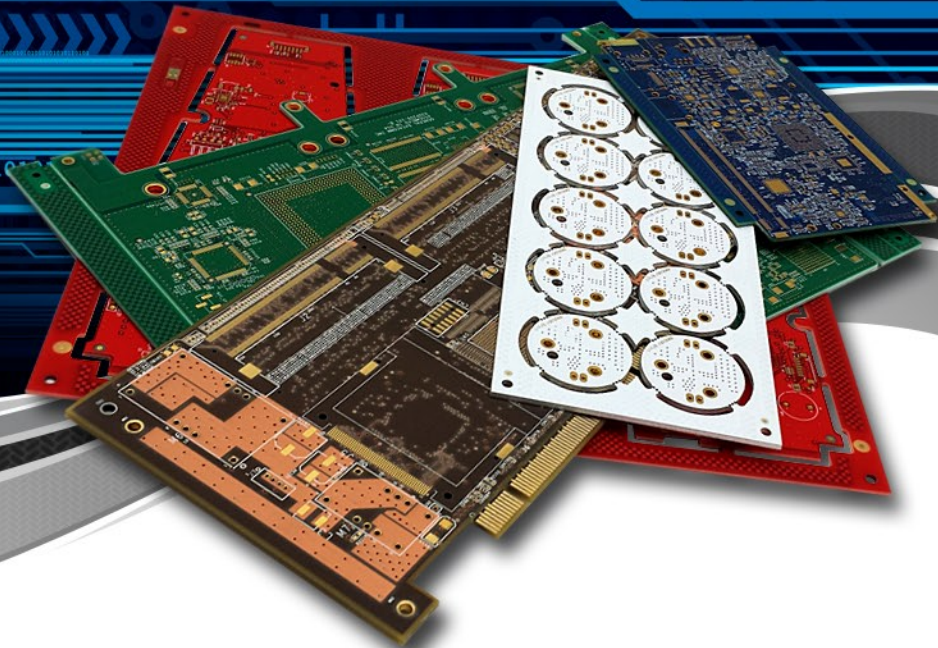
One way that engineers have traditionally reduced phonon scattering is to use high-quality materials that contain as few defects as possible. A more common solution, however, is to operate electronics in extremely cold conditions because scattering drops off dramatically when the temperature dips below about 50 kelvins, or about -370 degrees Fahrenheit.

"We don't know what the precise strategy will be yet, but now we know the direction we should be going. That's an improvement."



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# HDI PWB Reliability

by Paul Reid

An HDI PWB may be defined as a PWB with a higher wiring density per unit area than conventional PWB. They have smaller lines and spaces, smaller vias and capture pads and higher connection pad density than employed in conventional PWB technology. HDI boards utilize microvias, buried vias and sequential lamination with insulation materials and conductor wiring for higher routing density. HDI is an alternative to high layer-count and standard laminate or sequentially laminated boards.

HDI boards are characterized by high-density attributes including laser microvias, fine lines, smaller grid sizes and high performance thin materials. This increased density enables more functionality per unit area. Higher technology HDI PWBs have multiple layers of copper-filled, stacked microvias, which create a structure that enables even more complex interconnections. These very complex structures provide the necessary routing solutions for today's large pin-count chips utilized in mobile devices and other high technology products.

When it comes to HDI reliability, what we must do is consider two parts: the copper interconnects and the base material. What one can do is test the reliability with thermal cycling using Interconnect Stress Test (IST) coupons. The IST coupon tests the copper interconnection and checks for material damage. The coupon is fabricated on the production panel with the PWBs and has all the attributes of the PWB. So the coupon has the same construction, copper weights, hole sizes, grid sizes, and copper plating as is found in the corresponding board. The test thermal cycles the IST coupon, typically for 500 cycles, or until the coupon fails with a 10% increase in resistance due to cracks that develop in copper interconnections as a result of thermal cycling.

By measuring capacitance change between ground planes, we can determine if there is any significant material damage in the coupon. One must measure the capacitance in picofarads between adjacent ground planes before testing (to establish a base line), after preconditioning (a simulation of assembly and rework) and at the end of test. We then compare the measurement after preconditioning and at the end of test to



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## HDI PWB RELIABILITY *continues*

those original readings. A -4% change or greater indicates significant material damage and a cross section is processed to confirm or refute this finding.

The major problem is the implementation of lead-free soldering that requires assembly temperatures of 260°C. The FR-4 material is at its limit to withstand the heat when exposed to 260°C. The Z-axis expansion is at its highest at this temperature, putting extra strain on the copper interconnects.

The most common type of failure of a robust interconnection is a barrel crack that occurs in the central zone of the plated through hole (PTH). When tested using thermal cycling to 150°C, this is a wear-out type of failure that happens over

hundreds of cycles (500+ cycles). Surviving 500 cycles without any significant increase in resistance is considered a robust coupon.

In a weak coupon, the failure before 350 cycles may relate to a process problem, with the most common problem being thin copper plating. With thin plating, the barrel cracks may still be the cause the failure but it would be failing in less than 350 cycles. The PTH may also fail for corner cracks or interconnection separation.

Weak buried vias fail typically with barrel cracks in the center zone of the structure similar to PTHs and, less often, with corner cracks or interconnect separation. One of the HDI structures includes microvias stacked on buried vias.

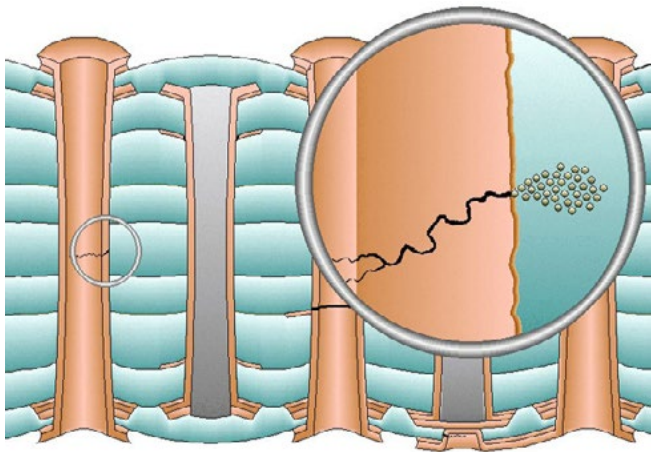


Figure 1: Barrel crack due to metal fatigue.

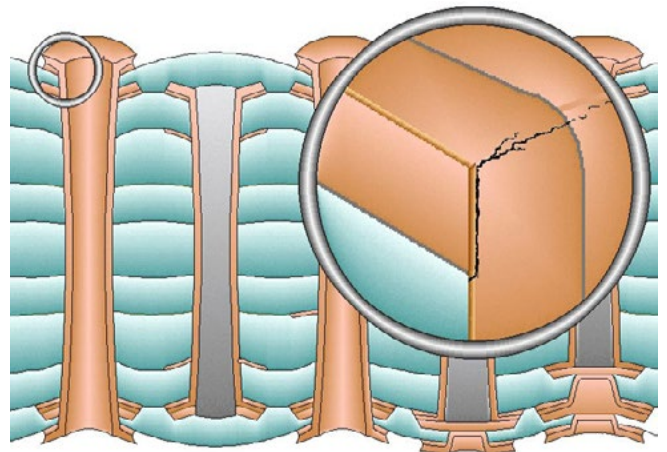


Figure 3: Corner or knee crack.

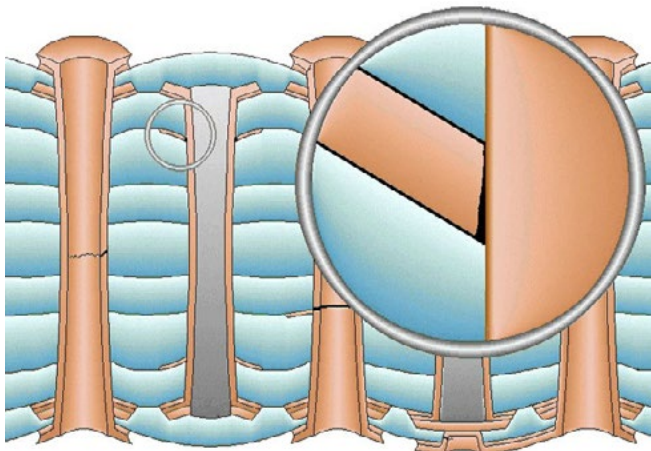


Figure 2: Interconnect separation.

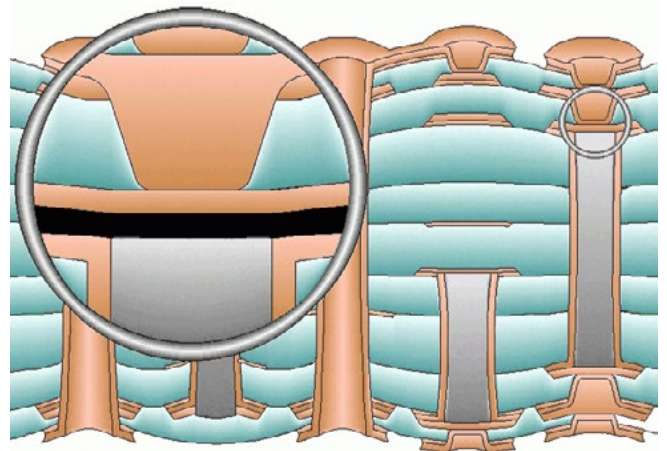


Figure 4: Lifted copper cap on buried via.



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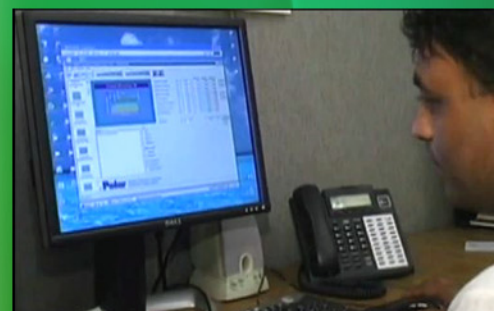
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**HDI PWB RELIABILITY** *continues*

In order to have a microvia stacked on top of the buried via, what we have to have is a conductive cap on the top of the buried via, which can also fail. There may be a separation of the copper cap from the top of the buried via or a crack in the cap of the buried via (Figure 7).

Microvias are typically the most robust type of interconnection. Because of their robustness, they are tested at 190°C. When tested at 190°C, robust microvias will survive 500 cycles while weak microvias will fail before 500 cycles. The most common cause of microvia failure is a separation between the base of the microvia and the target pad. The second most common cause of microvia failure is a barrel crack toward the base of the microvia. Other failure

modes include corner cracks (seen in copper-filled microvias) and pull out types of failures where the target pad cracks around the base of the microvia.

In HDI PWBs one must also consider construction. One may produce multiple microvias structures as either stacked or staggered. Microvias that are stacked are about four times more vulnerable to failure than the same structure in which the microvias are staggered. Well fabricated one- and two-layer microvias do not usually fail prematurely. Three- and four-stacked microvias tend to fail before 500 cycles when tested at 190°C and are a fabrication challenge.

The material damage is monitored in an IST coupon by measuring changes in capacitance

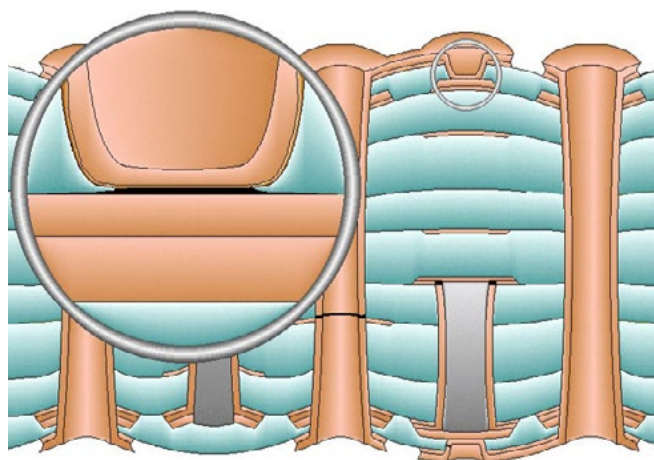


Figure 5: Microvia separation.

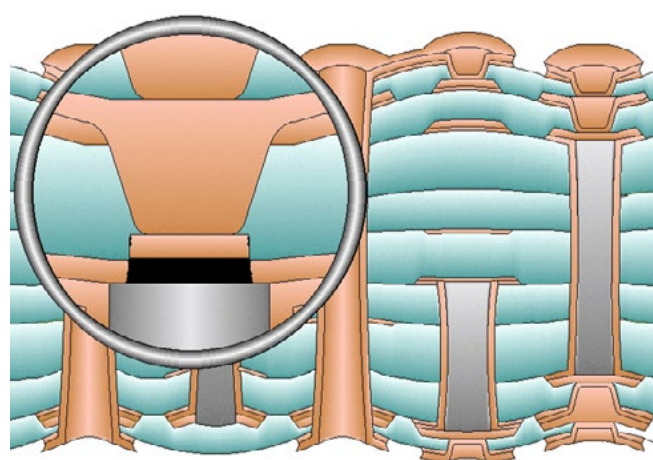


Figure 7: Microvia pull out failure.

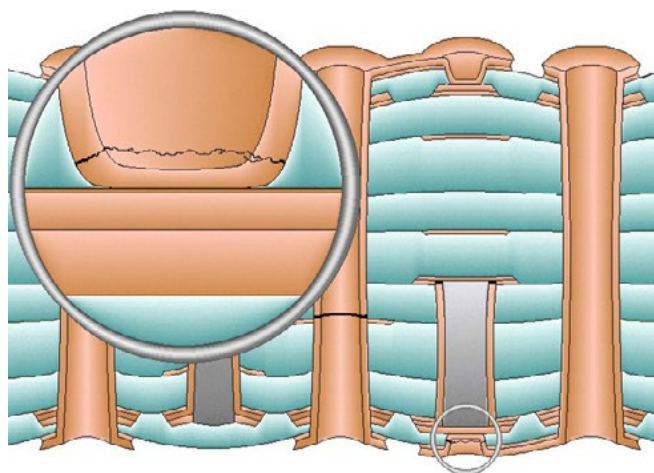


Figure 6: Microvia barrel crack.

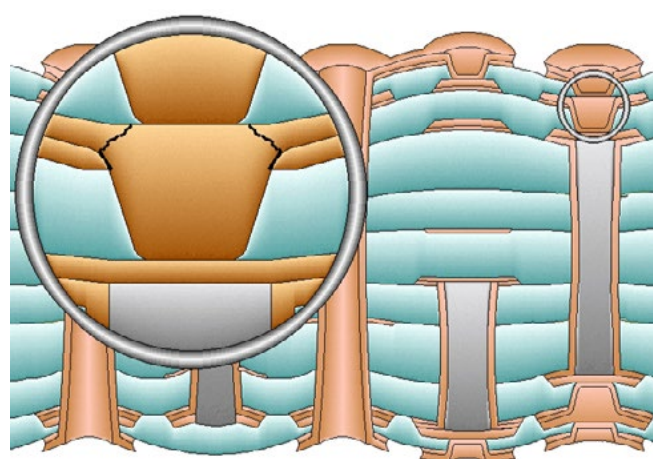


Figure 8: Microvia corner crack.





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MV = Microvia  
BV = Buried Via

## Microvia Constructions

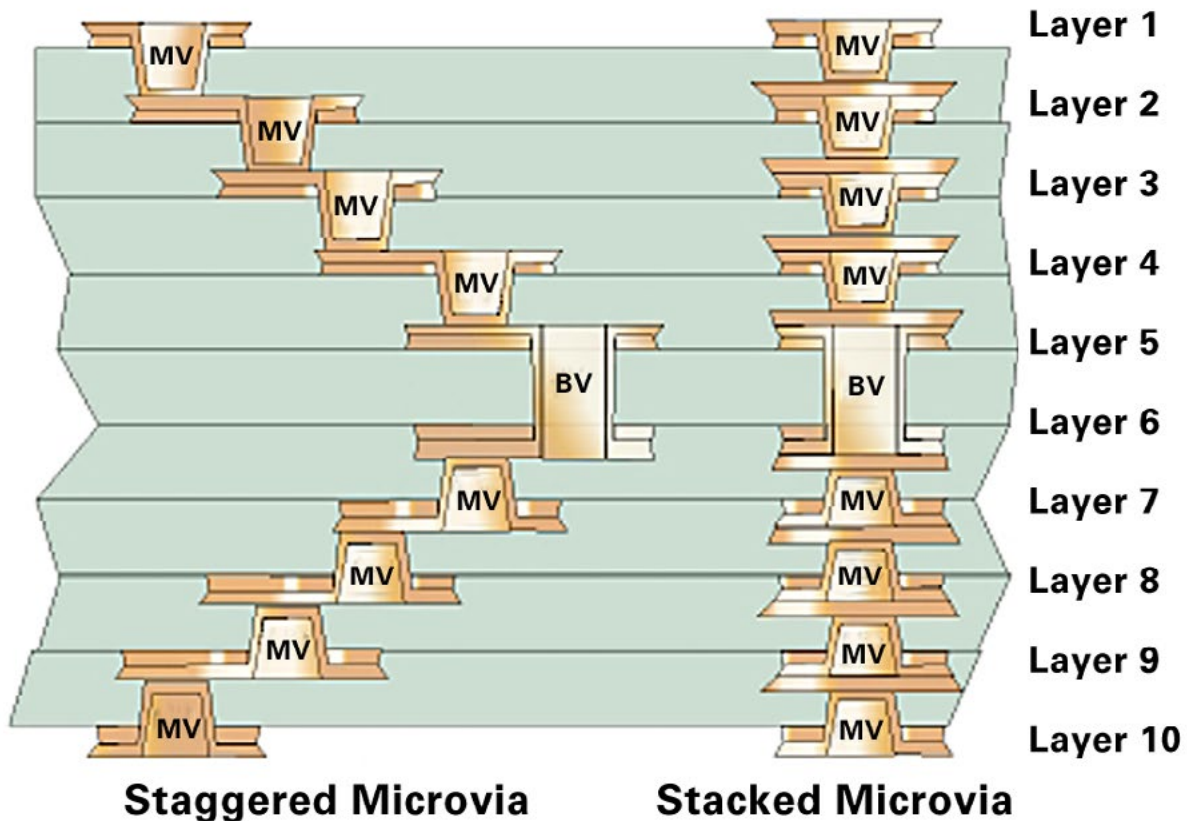


Figure 9: Staggered vs. stacked microvias.

between ground layers in the coupon. First, measure the capacitance between two flooded ground planes in the coupons in the as-received state and then again after the coupon has undergone preconditioning, and at the end of test. If there is significant material damage then a -4% or greater drop in capacitance is seen. To confirm the drop in capacitance is indicative of material damage, one or two of the coupons are subjected to a microsection to check for the presence of material damage.

The major types of material damage found are adhesive delamination, cohesive cracks, and crazing. Adhesive delamination is typically between two laminated surfaces like the b-stage, c-stage and copper interfaces. On occasion, adhesive delamination is seen between the glass

bundles as a group and epoxy of the dielectric. This type of failure is found typically on a 1 mm (.040") grid or greater.

The most common type of material damage is the cohesive crack, which is a crack that goes through the b-stage, c-stage and glass bundles. The cohesive failure is a breakdown of the epoxy system due to high temperatures of assembly. This type of failure is found typically on a 0.8 mm (.032") grid.

Crazing is the separation between glass fibers and the epoxy system. It looks like silver sheen on the glass bundles due to an envelope of air around the glass fiber. Crazing provides a pathway for conductive anodic filament (CAF) formation. This type of failure is found typically on a 0.5 mm (.020") grid.



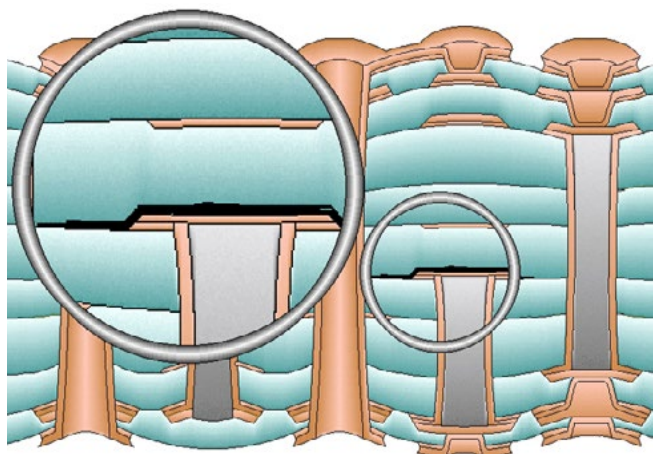


Figure 10: Adhesive delamination.

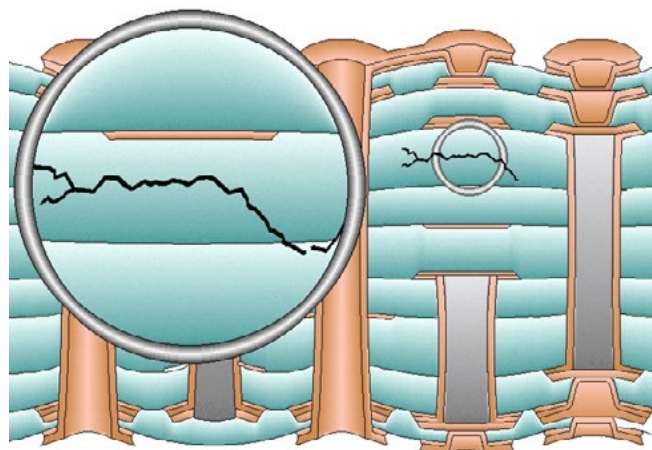


Figure 11: Cohesive crack.

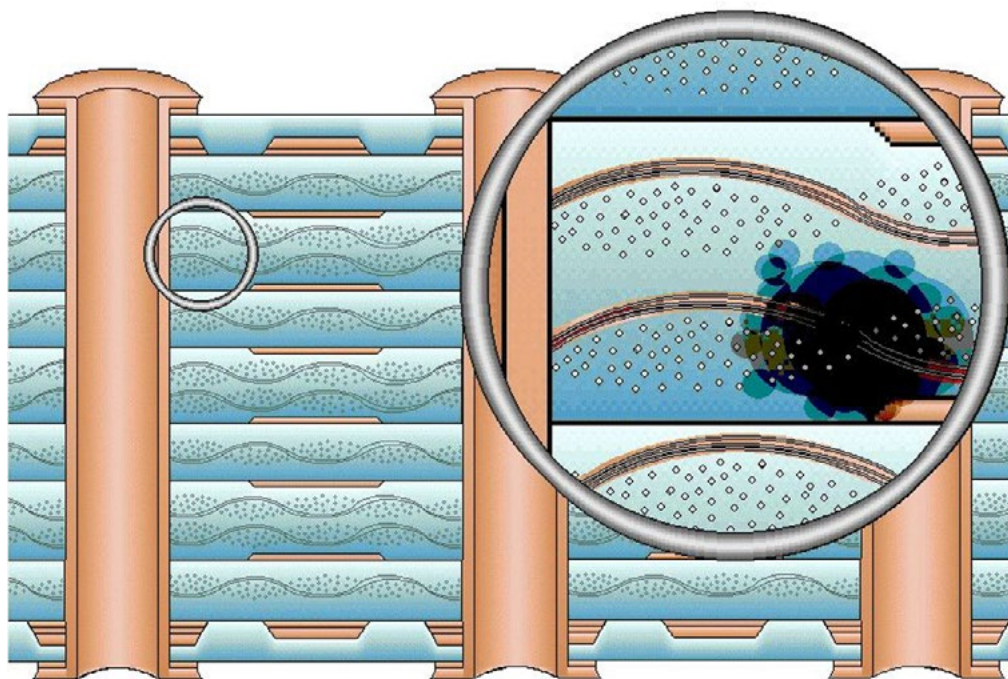


Figure 12: Craze with a CAF failure.

In conclusion, the use of HDI PWB reliability in lead-free applications is a dual-edged sword. The copper interconnections are more prone to a breakdown and the material is more prone to damage. That is not to say that robust PWBs cannot be made, but there is a challenge in producing them. One must test the interconnect and the material in order to confirm robustness in a given application. **PCBDESIGN**



Paul Reid's career in PCB fabrication and reliability testing spans 35 years. One of his specialties is producing technical animations of failure modes induced by thermal excursions, giving him insight into the mechanisms of circuit board failure. Reid is now retired. To contact the author, [click here](#).



# PCB007

## News Highlights



### **Viasystems' Faces Challenging Third Quarter**

"Regarding Viasystems' operating activities in the third quarter, we had to overcome several challenges, including a temporary work stoppage by employees in our largest factory in China, a sudden downturn of demand for products assembled in our Juarez, Mexico factory, and a temporary disruption in the supply chain for certain raw materials used to produce our printed circuit boards," says David M. Sindelar, CEO.

### **Dragon Circuits' Drone Division Experiments with Deliveries**

The company announces the successful completion of 14 autonomous and semi-autonomous delivery test runs with payloads ranging from a few ounces to a few pounds. With the recent interest in drone-based delivery by internet giants like Amazon and Google, Dragon Circuits looks to capitalize on a forthcoming demand with the expansion of their drone department.

### **TTM Reports Sequential Increase in Q3 Revenue**

Net sales for the third quarter of 2014 were \$345.3 million compared to \$297.6 million in the second quarter of 2014 and \$338.7 million in the third quarter of 2013.

### **Q3 PCB/EMS Market Snapshot**

I-Connect007's latest market survey—a one-minute survey designed to provide a snapshot of the current state of the PCB and EMS industries—offers a good sampling to give us a snapshot of where we've been and where we're headed.

### **IPC: N.A. September PCB Orders Strengthened**

"The North American PCB industry's solid sales and order growth over the previous month reflects normal seasonal patterns," said Sharon Starr, IPC's director of market research. "Despite strong order growth in September, orders continued to lag shipments by a small margin, pushing the PCB book-to-bill ratio just below parity."

### **MFLEX Rebounds in Q4, Expects Sustained Growth**

"We had a strong fiscal fourth quarter with net sales results at the high end of our guidance range, gross margin exceeding our guidance range, and a return to profitability, an important milestone for the company. Our net sales increased 32 percent sequentially, driven by new programs that ramped across our customer base," says Reza Meshgin, CEO.

### **AT&S Reports Improved Profitability in 1H of 2014/15**

In the first six months of the financial year 2014/15 (April 1–September 30, 2014) leading PCB manufacturer AT&S generated revenue of EUR 302.1 million, which was in line with the high level of revenue reported for the same period last year (H1 2013/14: EUR 299.9 million).

### **Continental Named PACE Award Finalists for BD-HDI PCB**

Continental, a leading international automotive supplier, has three product innovations advancing as finalists in the 2015 Automotive News Premier Automotive Suppliers Contribution to Excellence (PACE) Award program.

### **SCHWEIZER Posts Strong 3Q14 Results**

"Our business results after the first nine months of this fiscal year are really satisfying and come up to our expectations. In the third quarter, successes in our portfolio management already had an important influence on the improved results compared to the second quarter," says Dr. M. Schweizer, CEO Schweizer Electronic AG.

### **Aspocomp Reports Positive 2014 Amid Q3 Sales Drop**

Deliveries slowed down significantly in July–September, and third-quarter net sales amounted to EUR 4.9 million, a year-on-year decrease of EUR 0.3 million. Sales decreased mainly because telecommunication customers had placed over-large orders at the beginning of the year.



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# PCBs for Medical Applications—A Designer's Perspective

**by Kenneth MacCallum**  
STARFISH MEDICAL

*This article originally ran in the November 2014 issue of The PCB Magazine.*

## Introduction

PCBs are an increasingly important part of modern medical devices—especially electromechanical devices. The opportunities are large, but PCB designers and manufacturers must be aware of and work within the regulations and limitations in the medical device design process. This article will provide an overview of the medical device design process, the role of PCBs in that process and in modern medical devices, and include design considerations and tips for incorporating PCBs into medical devices.

## Medical Device Design Process

The medical device development industry is heavily regulated. Not only are the charac-

teristics and performance of the devices regulated, the design and development processes are as well. The focus is on well-defined and understood requirements, quantification of risk of harm to patient and operator, verification that the design meets the specifications and finally validation that the design is effective and safe.

Many medical devices are manufactured in lower volume than consumer electronics and have higher margins; and most have longer design cycles. Notwithstanding these differences, the technologies used in medical devices are often heavily leveraged from consumer electronics. This means the same creep towards higher density circuits and component packaging applies in the medical field. The same techniques of replacing wiring harnesses with PCBs and flex circuits that are found in consumer electronics are found in medical devices, although the drive towards these technologies may be increased reliability and reduced labour cost instead of decreased size and reduced parts cost.

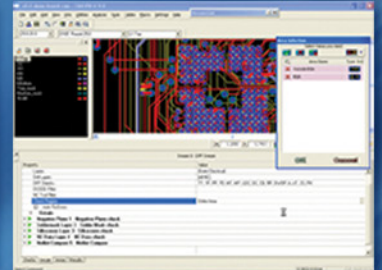
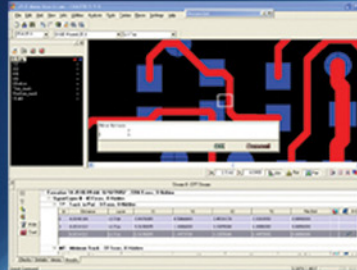


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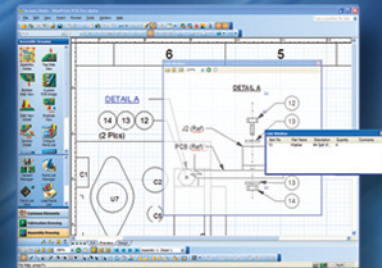
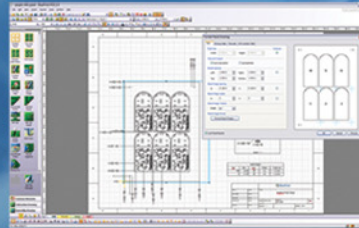
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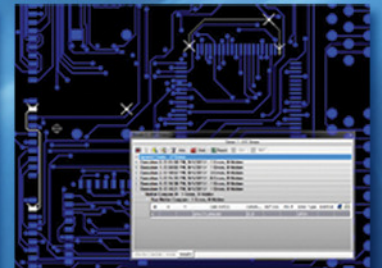
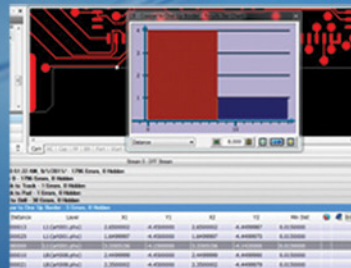
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PCBS FOR MEDICAL APPLICATIONS—A DESIGNER'S PERSPECTIVE *continues***Role of PCBs in Medical Devices**

Almost every medical device PCB is heavily influenced and constrained by the work of other disciplines. It is rare that a board can be designed without heavy consultation throughout the design cycle with mechanical engineers or industrial designers. There is usually no clear owner to the mechanical constraints of a PCB. A board outline may be proposed, then shoe-horned as the housing design gets hashed out. Rearranged as the main, large components, connectors and things get roughly placed; it will be tweaked again by the mechanical engineers or industrial designers. Finally the PCB designer will add their final touches and throw it back. This process is highly iterative and relies more and more on accurate 3D modeling of the board, connectors and wiring.

PCBs are structural elements with all sorts of great mechanical properties: they are fairly rigid, they're pretty strong and their tolerances are often excellent. The collaboration doesn't stop there either. Whoever is doing the firmware, software and logic design will also have some strong opinions about the board. It's best to get everyone together early and often to minimize the chance of later rework or worse.

Medical devices have some of strictest industry EMC requirements and regulations. Addressing these constraints is primarily achieved at the PCB level. This is yet another factor driving PCB density and manufacturing tolerances.

**Design Considerations and Tips**

As PCBs in medical devices become more complex and dense, it is more important than ever to ensure that the designs are correct and will function as required. Although a typical medical product will see three or more significant PCB design cycles it is important that the value of each cycle is maximized. The more functionality is designed into a board, the more possibilities for errors and faults there is.

**General Rules**

Electronic design automation (EDA) software now has sophisticated automatic design-rule checking, providing the rules are set up properly. These cannot prevent a bad design from getting into production, but they can prevent very common and frequent mistakes and oversights from getting out.

As PCBs get more complicated, it is helpful to partition designs hierarchically.

The top level of a hierarchical design is much like a block diagram of the board. Putting all connectors on the top level schematic sheet if possible, makes that sheet very useful during troubleshooting and design reviews. Child sheets encapsulate lower level functionality and sub-circuits. These can be referenced multiple times if a circuit is repeated, rather than cut and pasted as separate sheets. This allows for easier duplication of layout and is less prone to mistakes creeping in.

Once the schematic design is done, sub-circuits are often routed first, without constraining them to the board outline. This leads to a better overall layout compared to the traditional approach of component placement followed by routing. Once the sub-circuit layouts are routed, these are then pushed and shoved together like puzzle pieces. It is helpful to minimize the number of layers of sub-circuits even if the board will be manufactured with many. This makes it easier to re-use portions of layouts or adapt to last minute changes in layer counts.

More and more boards have high frequency differential pairs or impedance critical single-ended signals. Use a finite element analysis (FEA) calculator to determine the correct trace width and spacing. FEA gives more flexibility than the analytical solutions although they are often not far off each other. Do not neglect the effects of adjacent ground pours or traces. If you are unable to guarantee the impedance to the closest plane layer then adjacent ground pours are a nice way to control the impedance. Make sure

**“Once the sub-circuit layouts are routed, these are then pushed and shoved together like puzzle pieces. It is helpful to minimize the number of layers of sub-circuits even if the board will be manufactured with many.”**



to stitch the pour to the ground plane all along the controlled impedance traces. These calculations can then be compared with the controlled impedance results from the PCB manufacturer.

Unfortunately, the industry standard for PCB manufacturing files is still the old Gerber format. These files never contain quite enough information to be sure the boards will turn out right. They don't contain units, the decimal place can be ambiguous and even the origin is uncertain. It is good practice to disable zero suppression, and use an absolute origin for both Gerbers and drill files. It is also good practice to inspect all files with Gerber viewing software other than the EDA package that generated them. More and more PCB manufacturers now have automated workflows with little human intervention or interaction. Layer misalignment or scaling issues can sneak right through the manufacturing process and only be found when the boards are done.

### **Strategies for Planes and Pours**

It is a good strategy to flood planes rather than using single net planes. This provides the benefit of allowing the odd trace to route on that layer in a pinch. It also makes it easier to segregate power rails, separate planes and avoid interference with impedance controlled traces. Although it made sense in the days of limited file sizes and taped layouts to route planes as negatives, now this just seems like a source of errors either in review or manufacture.

Due to modern boards having many voltage rails, it is rarely advantageous or even possible to use complete power planes other than for ground. Instead, one or a few layers can be dedicated to power routing using fills and fat traces. As a bonus, signals can be snuck through on these layers as well. When pulling power off onto the component layers, it should first hit one or more bypass capacitors with the other pin drilled to ground, then the destination component pin.

Ensure flooded regions are stitched well to others. This is especially important on a two layer board where planes are impossible and ground is really just a collection of pours and is quite broken up. Pours should be kept away from controlled impedance traces unless they

are part of the controlled impedance strategy. If they are, then they should be well bypassed to ground. Note that impedance controlled traces crossing over fill boundaries will experience impedance discontinuities. These boundaries should be stitched either with vias to other layers or with bypass caps across the gap. This stitching should occur as close to the traces as possible.

It is often problematic to break planes into regions like analog signal ground or power ground. Having one good plane that is well decoupled to the chassis can be better than breaking planes up into different power regions. The effects and locations of high frequency switching currents should be carefully considered and controlled. If possible, keep them off the plane. If a plane must be broken into different regions, a line of no-fit caps should be added, just in case.

Consideration should be given to the currents of various sub-circuits that will flow through the plane and their impact on other subcircuits along the way. A slight void or cut in the plane to explicitly corral these currents can be an effective strategy to control them. Sometimes a different arrangement of sub-circuits will give even better results.

### **Layout EMC Considerations**

Given that medical devices are heavily regulated, at some point electromagnetic compatibility will have to be considered. Add ESD & EMC reduction components like TVS diodes and ferrites, even if the board is a prototype with no plans for EMC testing. This provides a head start to flush out problems early. It also plans ahead for a prototype being used beyond what was initially imagined or intended. Consider designing in the parts without populating them right away. Then they can be easily added later without cutting and gluing.

Consider where noise may come from both on and off of the PCB. Reducing noise at the source is always a better strategy than combating it only where it is creating trouble. An example of this is the high speed parallel lines to a TFT display. A tidy bank of ferrites right at the driver outputs is often all it needs. This is easiest done at the PCB design stage.

**PCBS FOR MEDICAL APPLICATIONS—A DESIGNER'S PERSPECTIVE** *continues*

When laying out switch-mode power supplies or filters on PWM circuits, designers should think about high-frequency current paths—there are usually two of them—and keep the area of these paths minimized. This usually means placing the big components first: switches, inductors, caps and diodes.

Only connect switch-mode supply and PWM filter circuits to the rest of the PCB ground in one place. This includes signal grounds to the control ICs. Use the ground terminal of the main input capacitor. If the connection is done in more than one location, the ground plane and hence other circuits may be polluted with switching currents. Be wary of nearby copper pours accidentally touching the ground net somewhere else.

### **Simulation**

Given the investment in time and effort to design PCBs it pays to simulate in order to learn as much as possible prior to the board order. Usually this does not mean simulating a whole circuit but focuses on key sub-circuits, or even key components of these sub-circuits.

A good candidate for simulation is to validate the choice of switch-mode power supply inductor. If the inductor is poorly chosen the circuit will smoke. Typical equation-based methods for determining the peak current requirements often are optimistic. A quick simulation regularly shows that under certain conditions the current will go just a bit higher. Simulate at worst-case conditions: maximum current, minimum inductance, maximum input voltage, etc. This determines the peak inductor current, which is often much higher than expected.

Simulation is also very useful in developing feedback systems. In medical devices it's not unusual for a control system to have hundreds of Watts at its disposal. To rush to experimentation in such a system is likely to result in damaged parts or even injuries

Use Spice, MATLAB, FreeMat or even a spreadsheet to numerically model the behavior of a system, particularly an electronic or electromechanical one. This method allows detailed exploration of system performance over a wide range of conditions prior to building a prototype. It is especially useful to test conditions that occur infrequently or ones you can't easily replicate with the available test equipment.

Note that simulation results are often incorrect. Simulation models are frequently wrong, incomplete or inappropriate for a particular purpose, whether they are made from scratch or they are from an existing library or even a manufacturer's website or datasheet. Models rarely take into account actual physical limitations. One can get valid looking simulation results from a situation which would vaporize parts in a microsecond. Similarly, the system modeled might ignore a part's non-ideality or a parasitic signal path that occurs in reality and critically affects performance.

It is useful to think of simulation like physical breadboarding. The same thought processes that would be used as physical components are wired up in the lab and the critical thinking that happens right before turning on the bench power supply are helpful during simulation. Special attention should be paid to the operating parameters being simulated and how the parts would behave in those conditions, especially with respect to their absolute maximums. Simulation complements real lab experimentation: model it, make it and repeat as necessary.

### **Prototyping**

Even after simulating a system, it is important that it be physically prototyped. Frequently a key part or characteristic of a system is found to be missing once it is soldered together and scoping begins. In that case, an iterative process

“  
***One can get valid looking simulation results from a situation which would vaporize parts in a microsecond. Similarly, the system modeled might ignore a part's non-ideality or a parasitic signal path that occurs in reality and critically affects performance.***  
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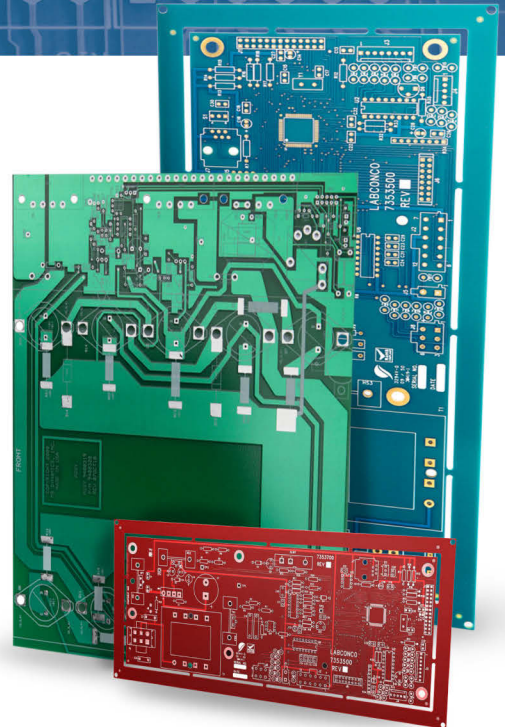


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## PCBS FOR MEDICAL APPLICATIONS—A DESIGNER'S PERSPECTIVE *continues*

of simulation, circuit changes, tests and measurement may be required.

A recent challenge in breadboard testing and early prototyping is the steady industry shift towards higher density packaging and higher pin counts. Many components are nearly impossible to physically prototype with using traditional bread-boarding techniques. How then can sufficient testing and prototyping occur prior to the onset of detailed product design?

Fortunately, a new class of PCB manufacturers has stepped into the market. It is now possible to buy just a handful of high-quality, custom PCBs for less than the cost of the prototyping supplies and time that would have been required for bread-boarding. These manufacturers create opportunities for board layout that were not imagined just a few years ago. It is now possible and economical to make boards for extremely early prototypes. This ability used to be solely available to companies with large budgets or specialized equipment. This change in the PCB manufacturing

market will have a significant impact on medical device development.

### Conclusion

The medical device industry is a heavily regulated industry with slightly different motivations than consumer electronics. Many of the same design strategies apply and many similar technologies are leveraged. PCB design and use in this industry are growing in sophistication and precision. Similarly, advances in manufacturing capabilities, such as low volume, low cost, quick-turn PCBs are being embraced and leading to noticeable shifts in the design and development process. **PCBDESIGN**



Kenneth MacCallum is principal engineering physicist at Starfish Medical.

## video interview

### R&D and High-Tech Applications Set OEMs Apart

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Anaya Vardya, CEO of American Standard Circuits, discusses how his company sets itself apart from the rest by focusing on R&D, and providing R&D services for their customers. Recently, the company has been researching sputtering copper into aluminum-backed PCBs with blind vias.



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# Signal Integrity, Part 3

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD

In last month's [column](#), I looked at the effects of crosstalk, timing and skew on signal quality. This month, I will continue to discuss signal integrity, in particular where most designers go wrong and how to avoid the common pitfalls.

Digital designs become less forgiving as edge rates and frequencies increase. What used to work in the past may not work now, and a different approach to layout may be necessary. Also, there may be many issues that aren't at first apparent, but affect the reliable performance of the product. Signal and power integrity issues, for instance, often manifest themselves as intermittent operation, which can be very difficult to nail. So it is best to find these issues during the design process and eliminate them at the source, rather than apply a Band-Aid solution after production.

I have analyzed many high-speed boards over the past 15 years and have established a process that I follow in order to achieve effective, consistent results. Not all assessments require expensive analysis tools, but rather common sense. I find that a large percentage of issues can be detected just by eye-balling the design—simulators don't pick up everything.

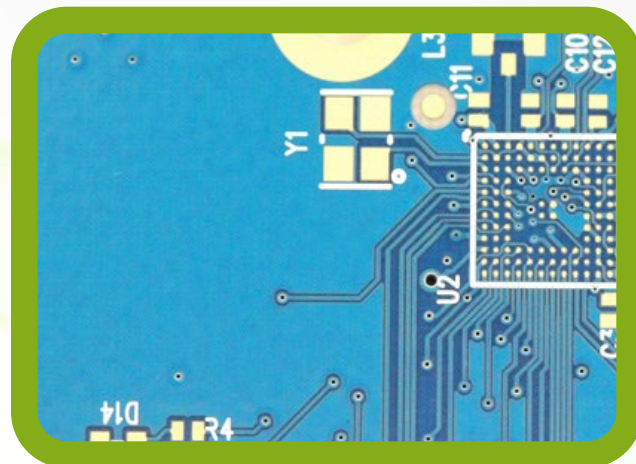
The first thing to look at, of course, is the board stackup. The substrate is the most important component of the assembly and needs to be planned correctly in order to maintain consistent impedance across layers, avoid unintentional signal coupling and reduce electromagnetic emissions. In Part 1 of this series, I set out the basic rules for stackup planning that should be adhered to. The most important being: All signal layers should be adjacent to, and closely coupled to, an uninterrupted reference plane.

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Z <sub>0</sub> )	Edge Coupled Differential (Z <sub>diff</sub> )	Broadside Differential
1	8 4 8	Soldermask		Liquid Photoimageable	3.8	0.5							
2		Signal	Top	Conductive			2.2	8	4	0.43	53.5	98.11	
3		Prepreg		370HR; 1080; Rc= 66% (5GHz)	3.72	2.9							
4		Plane	GND	Conductive			0.7						
5		Core		370HR; 1-1652; Rc=43% (5GHz)	4.2	5							
6		Signal	Inner 3	Conductive			0.7	8	4	0.19	54.03	101.32	
7		Prepreg		370HR; 7628; Rc= 50% (5GHz)	4.05	8							
8		Plane	VDD	Conductive			0.7						
9		Core		370HR; 3-7628/1080; Rc=44% (5G...	4.2	24							
10		Plane	VSS	Conductive			0.7						
11		Prepreg		370HR; 7628; Rc= 50% (5GHz)	4.05	8							
12		Signal	Inner 6	Conductive			0.7	8	4	0.19	54.03	101.32	
13		Core		370HR; 1-1652; Rc=43% (5GHz)	4.2	5							
14		Plane	GND2	Conductive			0.7						
15		Prepreg		370HR; 1080; Rc= 66% (5GHz)	3.72	2.9							
16		Signal	Bottom	Conductive			2.2	8	4	0.43	53.5	98.11	
17		Soldermask		Liquid Photoimageable	3.8	0.5							

Figure 1: Substrate with each signal layer adjacent to a reference plane.



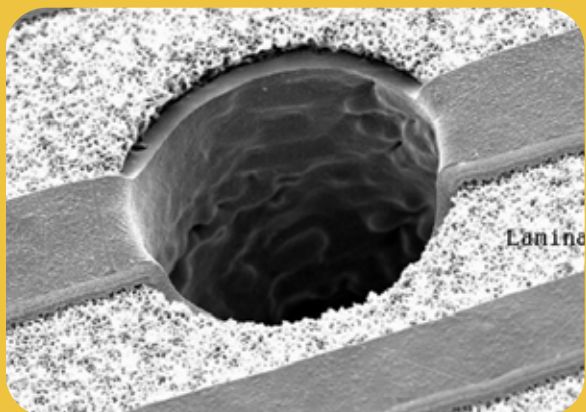
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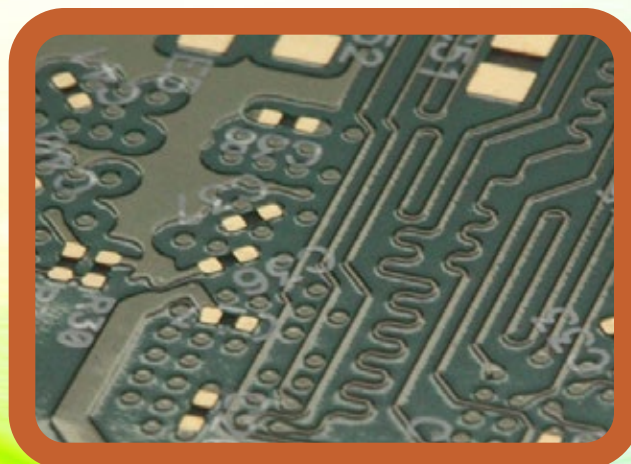


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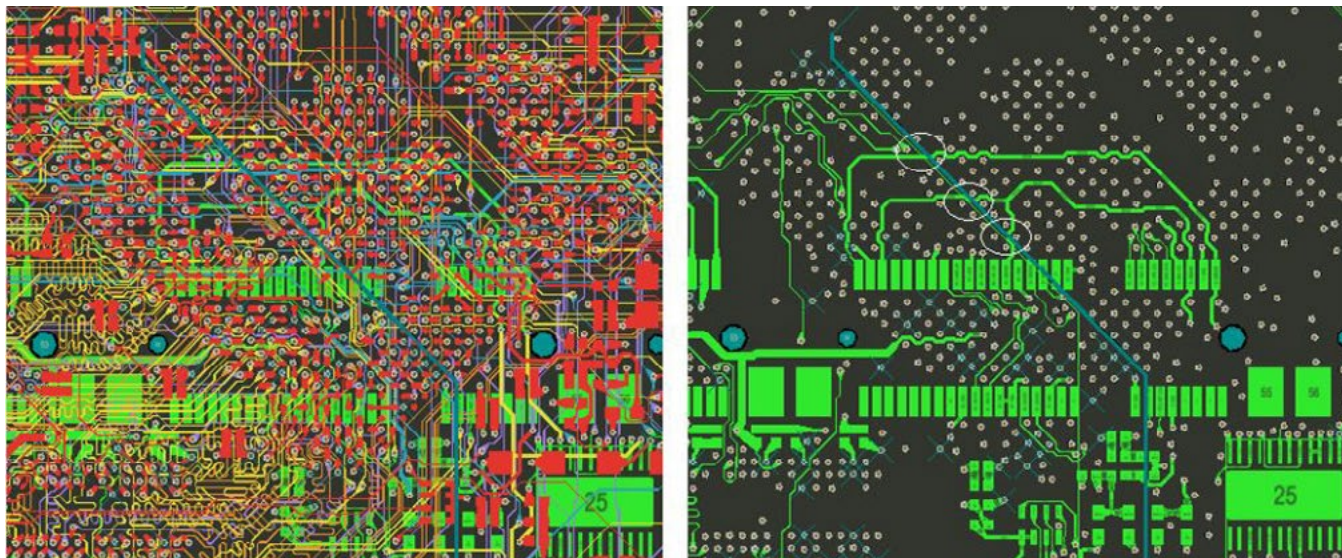
**SIGNAL INTEGRITY, PART 3** *continues*

Figure 2: Multiple signal layers (left), bottom layer and adjacent plane (right).

creating a clear return path and eliminating broadside crosstalk. Figure 1 illustrates a good stackup in this regard.

This brings us to the next issue: split planes and current return paths. With all signal layers turned on in your layout tool, it is difficult to see the wood for the trees. Figure 2 illustrates the dense routing of multiple signal layers viewed together (left)—confusing to the sharpest eye—and the bottom layer, with the adjacent plane (right). The best way to simplify this view is to determine which copper plane (either ground or power) that each signal layer is referenced to. Turn on that signal layer and plane layer to view simultaneously. You can then easily see traces crossing split planes. In this case, the thick traces are power so it is of little consequence. But, this could well be disastrous if a high-speed signal was to cross the split. This not only presents a signal integrity issue, but will generate extreme amounts of common-mode currents, which typically flow out I/O cables and cause electromagnetic compatibility failure.

If digital signals must cross a split, in the power reference plane, a quick fix is to place one or two plane decoupling capacitors (100 nF) close to the offending signals. This provides a path for the return current between the two supplies (e.g., 3.3 V —||— 1.5 V). Al-

ternatively, if GND planes are used for the current return, then GND stitching vias should be placed close to each layer transition (via) to create a clear path for the return current. Fortunately, most high-speed designs have numerous decoupling capacitors that can usually provide the return path, without the addition of stitching vias.

Crosstalk can be coupled trace-to-trace, on the same layer, or can be broadside coupled by traces on adjacent layers. The coupling is three-dimensional. Traces routed in parallel and broadside cause greater amounts of crosstalk than those routed side by side. This is due to the width of the trace being much larger than the thickness, so more coupling occurs in the broadside configuration. Figure 3 shows how the coupling is increased in the broadside configuration (top). You can see the electric fields coupling between the traces and planes.

Also, these days many stackups use buildup microstrip layers top and bottom of the board. This can be very dangerous as one needs to take particular care of crosstalk caused by traces routed on the adjacent layers.

In Figure 4, the red lands are on the top layer and the yellow signal trace in one layer 2. The yellow trace goes directly beneath the top land and the high-speed signal is coupled to the land due to the extremely close proximity (3.4 mil)



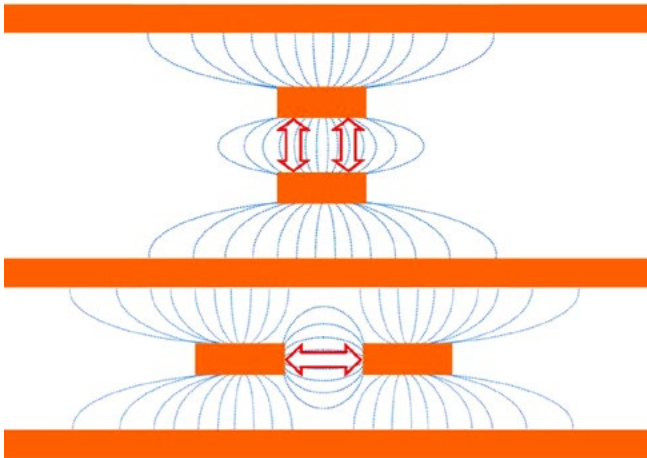


Figure 3: Broadside coupling (top) compared to edge coupling (bottom).

of signal layers. Figure 5 shows part of the stack-up cross-section in the ICD Stackup Planner. In this case, both signal layers are referenced to the GND planes on layer 3.

Recently, I analyzed a design where the lands on the top layer connected to a WiFi module and the signal on layer 2 injected a random pulse into the module via this close coupling. The symptom was that the product ran for about an hour then all of a sudden missed a beat and had to be rebooted. Once this issue was fixed, the product then ran reliably for days without failure. Simple fix, but hard to find!

Crosstalk is also typically picked up on long parallel trace segments. These can be on the same layer or may also be broadside coupled from the adjacent layer. Fortunately, source synchronous busses have a unique immunity to crosstalk, provided that the ringing has settled by the time the bus is sampled by the clock. So there are two issues here:

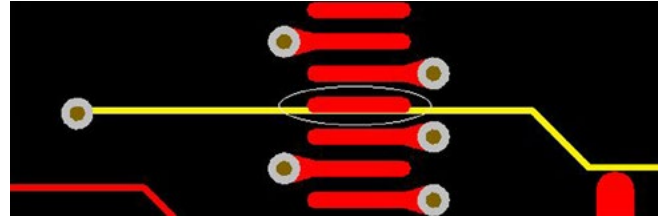


Figure 4: Buildup microstrip layers—layers 1 and 2.

1. Keep parallel trace segments as short as possible to reduce coupling (crosstalk) unless you are using a synchronous bus. Space the groups of signals (e.g., address and data) by three times the trace width.
2. Always route the clock (or strobe) to the longest delay of the group of signals. This allows the data to settle before it is read by the clock.

In a previous column, [Matched Length Does Not Always Equal Matched Delay](#), I discussed matched length routing and how matched length does not necessarily mean matched delay. Flight time (propagation delay) varies depending on the dielectric material that the signal propagates in.

$$\text{Flight Time} = \frac{\text{Length} \times \sqrt{\text{Er eff}}}{c}$$

Eq. 1

Where  $c$  is the speed of light and “Er eff” is the effective dielectric constant.

In a microstrip configuration, the effective dielectric constant is dependent on the FR-4

8/21/2014													
Total Board Thickness: 69.4 mil													
Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdiff)
1	0 4 0	Soldermask	Top	Dielectric	3.3	0.7	2.2	10	5.5	0.55	70.13	121.01	
2		Prepreg	Inner 2	Conductive	3.7	3.4	0.6	10	4.5	0.18	53.5	99.23	
3		Signal	Core	Dielectric	3.6	3	0.6						
		Plane	GND	Conductive			0.6						

Figure 5: Layers 1 and 2 have only 3.4 mil separation and are prone to coupling.

**SIGNAL INTEGRITY, PART 3** *continues*

material, the solder mask and the air above. In a stripline configuration, it is dependent on the FR-4 material above and below the trace. So, microstrip signals tend to travel faster than stripline as the effective  $\epsilon_r$  is smaller. Also, an accordion or serpentine pattern will be faster than the equivalent straight trace, due to forward crosstalk. So this is not a simple calculation and requires a simulator to compare delays on different layers of the substrate.

Rather than matched length, one needs to compare the actual delay as the signals propagate through different materials in the substrate. This is done in order to determine the skew between clocks (or strobes) and the groups of signals they control. If you must assess using matched length, tighten the tolerance as this will still reduce the skew.

Routing critical signals between the planes can reduce emissions by 10 dB or more. There are four constraints to keep in mind:

1. Keep the mark-to-space ratio of the waveform equal as this eliminates all the even harmonics.
2. Route high-speed signals out from the centre of the board where possible, as any radiation will be in the opposite direction and will tend to cancel.

3. Route high-speed signals between the planes, fanout close to the driver (200 mils) dropping to an inner plane and route back up to the load again with a short fanout.
4. Use the same reference plane for the return signals, as this reduces the loop area and hence radiation.

Embedding signals between the planes also reduces susceptibility to radiation, as well as providing ESD protection. So, not only does this prevent noise from being radiated, but it also reduces the possibility of being affected by an external noise source.

In Figure 6, the noisy waveform produces high levels of electromagnetic emissions. With a maximum radiation of 56.94dB @ 7.5GHz, this well exceeds the FCC/CISPR Class B limit. Generally, this is due to unterminated transmission lines, excessive crosstalk or too much driver strength. Possible solutions to try are:

1. Reduce the driver current to the medium strength of 8mA.
2. Check for crosstalk, particularly on long segments.
3. Add series terminators.

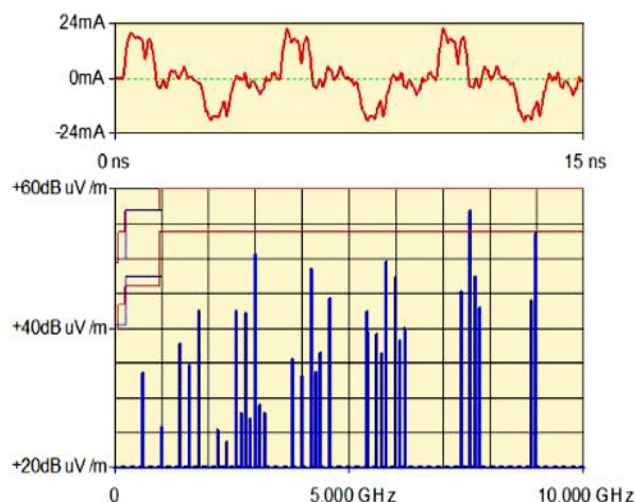
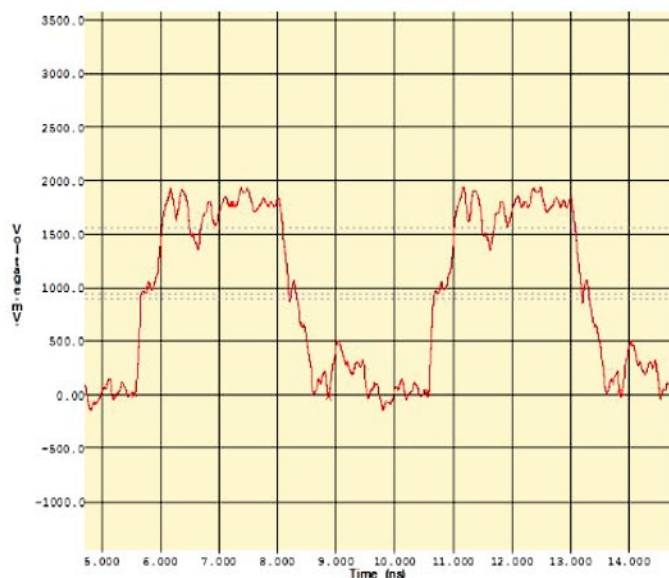


Figure 6: Noisy waveforms increase radiated emissions.



Placing series terminators from the beginning will not hurt, as they can always be replaced by zero ohm resistors if not needed—not a great expense, but this can alleviate ringing problems. Terminators do however slow down the signal rise time.

If this noise is not constrained, at the source, then it will be coupled into nearby victim traces (crosstalk) and radiate to create more EMI. Apart from the issues of EMI, signal integrity and crosstalk, this noise can cause intermittent operation of the product due to timing glitches and interference, dramatically reducing the products reliability.

### Points to Remember:

- Digital designs become less forgiving as edge rates and frequencies increase.
- Signal and power integrity issues, for instance, often manifest themselves as intermittent operation.
- The first thing to look at is the board stackup. All signal layers should be adjacent to and closely coupled to an uninterrupted reference plane, creating a clear return path and eliminating broadside crosstalk. Figure 1 illustrates a good stackup in this regard.
- The best way to simplify a complex view is to determine which copper plane (either ground or power) each signal layer is referenced to. Then turn on that signal layer and plane layer to view alongside.
- If digital signals must cross a split in the power reference plane, decoupling capacitors can be placed close to the offending signals to provide a path for the return current between the two supplies.
- If GND planes are used for the current return, then GND stitching vias should be placed close to each layer transition.
- Crosstalk can be coupled trace-to-trace, on the same layer, or can be broadside coupled by traces on adjacent layers.
- Traces routed in parallel and broadside cause greater amounts of crosstalk than those routed side by side.
- Buildup microstrip layers can be very dan-

gerous, as one must take particular care of crosstalk caused by traces routed on the adjacent layers.

- Keep parallel trace segments as short as possible to reduce coupling crosstalk.
- Always route the clock to the longest delay of the group of signals. This allows the data to settle before it is read by the clock.
- Flight time varies depending on the dielectric material that the signal propagates in.
- If you must use matched length, tighten the tolerance as this will still reduce the skew.
- Routing critical signals between the planes can reduce emissions by 10dB or more.
- Embedding signals between the planes, also reduces susceptibility to radiation, as well as providing ESD protection.
- To avoid noise on waveforms, reduce the driver strength to the medium current, check for crosstalk, particularly on long segments, or add series terminators.

### PCBDESIGN

### References

1. Barry Olney: [Beyond Design: Practical Signal Integrity](#); [Beyond Design: Pre-Layout Simulation](#); [Intro to Board-Level Simulation and the PCB Design Process](#); [Beyond Design: Impedance Matching: Terminations](#); [Beyond Design: Matched Length Does Not Always Equal Matched Delay](#)
2. Howard Johnson: [High-Speed Signal Propagation](#)
3. The ICD Stackup and PDN Planner are distributed globally by [www.altium.com](http://www.altium.com)



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, [click here](#).

# Sketch Routing, Part 3: Performance

by **Charles Pfeil**  
MENTOR GRAPHICS

This is the third and last article in a series discussing the core elements of effective PCB routing (control, quality, and performance). I recommend reading the [August](#) article on control and the [October](#) piece on quality, because they provide background information that will help when reading this article.

The primary attraction with autorouting compared to manual routing is the speed. In the previous articles, I emphasized the fact that user control, quality and performance are all required for a successful routing environment. Most autorouters are incredibly fast; but if the quality is lacking, the results require too much editing. When the quality is poor, the time to

clean up the routing results is sometimes more than it would be to manually route it from the beginning. The sketch router provides the designer with performance that is normally only associated with autorouting while at the same enabling user control and route quality.

What is it about the sketch router that enables high performance compared to manual routing? There are two factors: escape optimization and multiple netline routing.

## Escape Optimization

With BGAs and large connectors, hundreds and sometimes thousands of netlines run between them. If the BGA is an ASIC or an FPGA

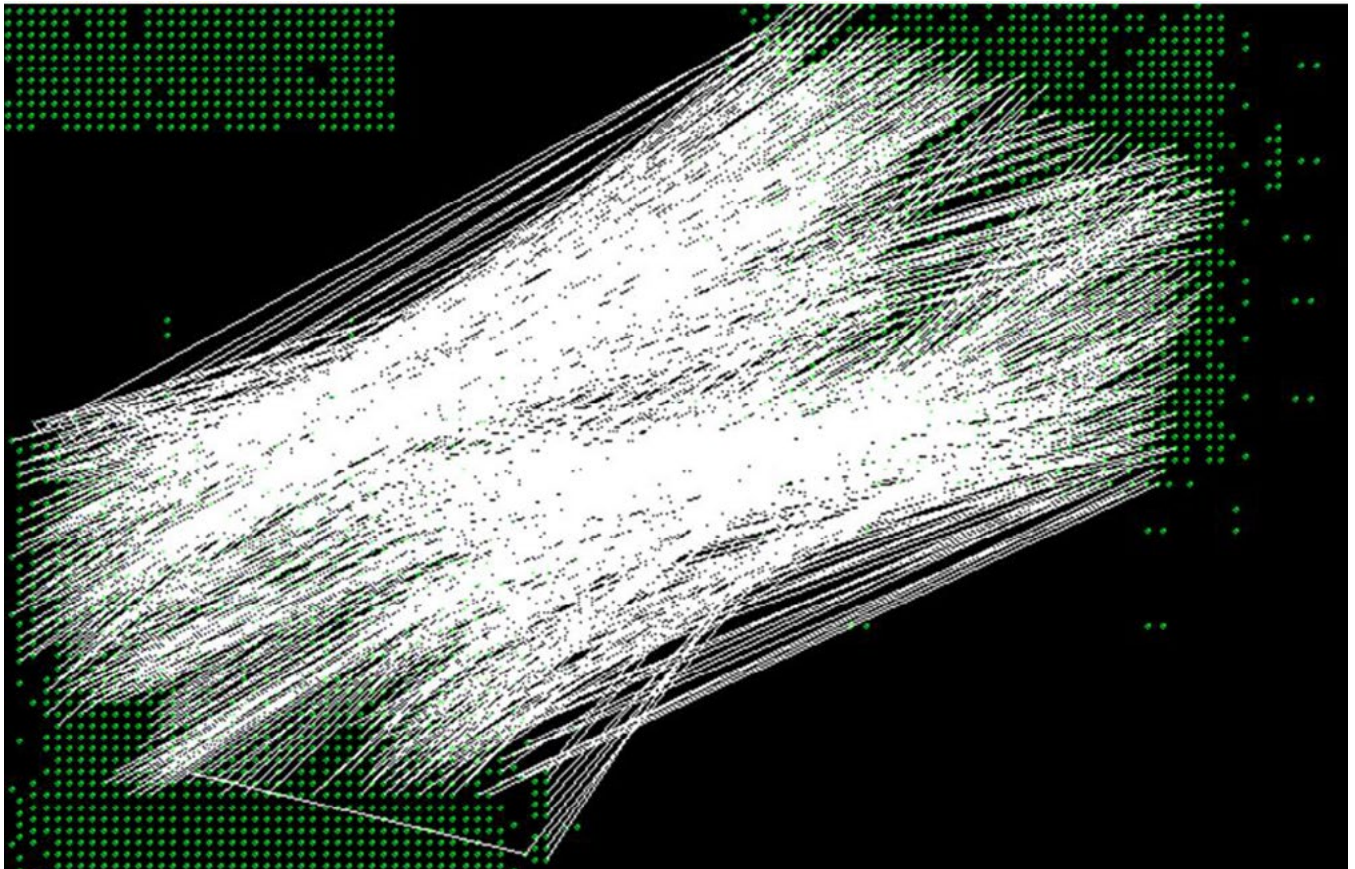


Figure 1: Tangled netlines mean a difficult routing challenge.



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## PART 3: PERFORMANCE *continues*

without pin optimization for routing, it is a very complex routing problem due to the sheer volume of netlines that cross each other (you can see the mess in Figure 1). When manually routing designs like this, trying to find a way to route these netlines so they don't block each other is the most difficult part.

When manually routing starting with one BGA, the routes can be escaped from the fanouts to the edge of the component in a fairly orderly manner, adding them one-by-one or using MultiPlow to do a group of them. It is not too difficult to fill up all the channels on each layer with optimal escape routing at the start. The problem occurs when getting to the target component(s). Routing into a BGA with non-optimized netlines presents a significant problem. Now the routes are nicely ordered, but the netlines cross in a manner that can only be described as a mess.

The initial netlines can be routed into the BGA fairly easily, but as more and more are routed, meandering is required to complete them.

It isn't long before the meandering traces block other routing and there are no more channels for new traces. I estimate from my experience that about 30% of these routes need to be unrouted and started in a different direction at the beginning to find an open channel all the way to the target pin or via.

This re-route of failed route paths is the greatest contributor to slowing down the routing task. Even rerouting from a different direction at the start doesn't necessarily ensure that the route can be completed. It is a difficult and sometimes frustrating task. Often, additional vias are required to complete the routing. Of course, if pin swapping or automatic pin optimization is allowed and applied, the routing challenge is less daunting; yet this kind of preparation for making routing more direct is not always allowed.

What does the sketch router do with escape optimization that makes such a difference? When considering the set of netlines to route, the sketch router will simultaneously escape the

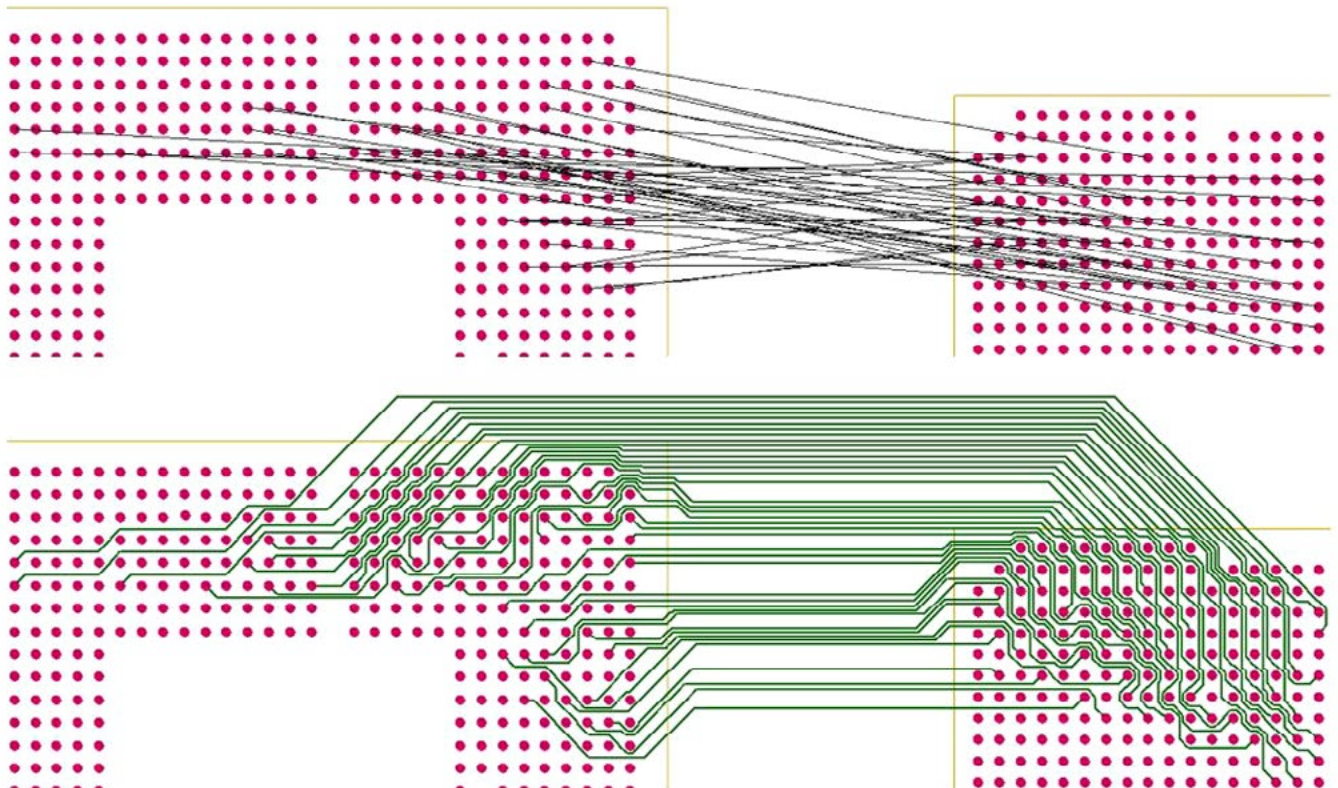


Figure 2: Sketch router escape optimization of tangled netlines.



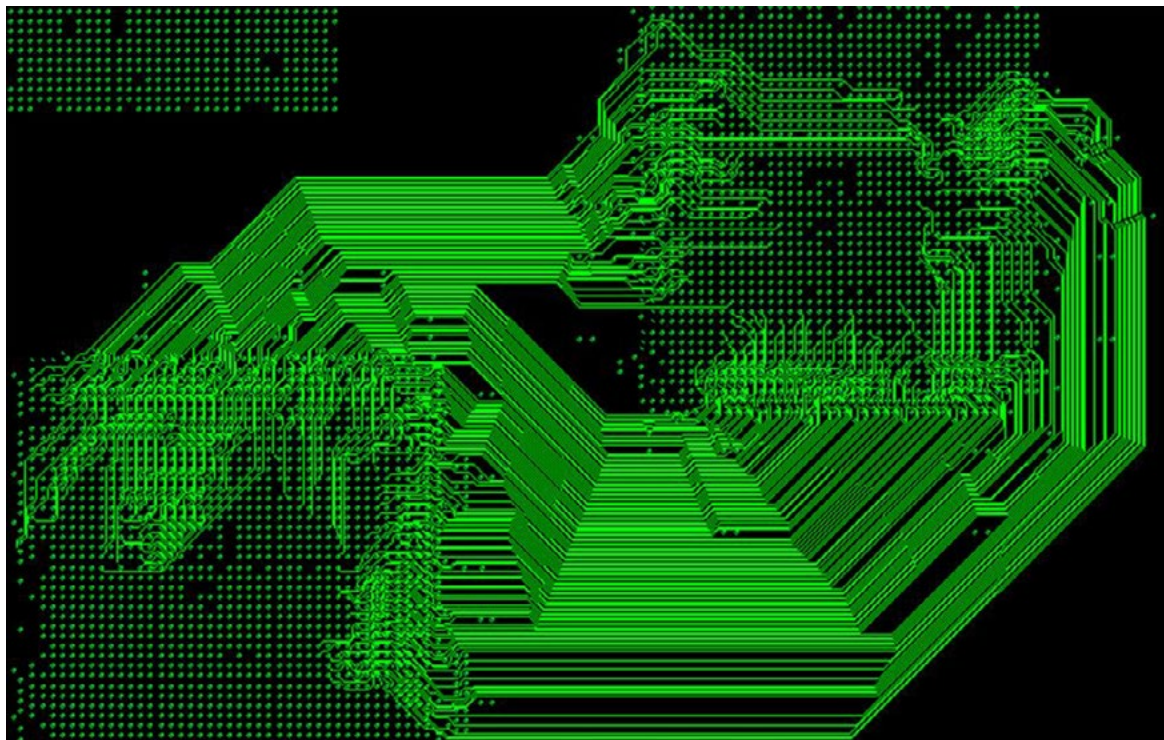


Figure 3: Sketch router on one layer, routing 151 netlines in 6.5 minutes.

two ends of the netlines out of the BGAs or connectors (or any other components for that matter) and order them in a manner that enables completion of the routing without additional vias. It is an approach that makes an incredible difference in performance. Note the example in Figure 2. The routing looks clean, but the ordering of the traces required to route without vias is not simple.

### Multiple Netline Routing

The second aspect of the sketch router that enables high performance is the fact that it can consider routing from one to hundreds of netlines at the same time. One example I recently did was to route 765 netlines between two BGAs. I used six layers, and using a number of different sketch paths, it routed 650 of them in 18 minutes. Each time the sketch router is used, it attempts to route all the selected netlines and if it fails, they remain selected and the sketch router can be used to route them on the next layer, even reusing the previous sketch path if desired. Keep in mind, this routing was accomplished without any extra vias other than the

existing fanout vias. Figure 3 is an example of this routing on one layer.

How long would it take you to route 650 netlines on six layers using only fanout vias?

### Video Examples

As with the previous two parts of this series, we've published a video on YouTube that will give you a much better idea of the performance than still illustrations can. [Click here](#) to watch.

#### PCBDESIGN



Charles Pfeil is an engineering director in the Systems Design Division at Mentor Graphics. He was the original product architect for Xpediton PCB and an inventor of XtremePCB. Pfeil has been in the PCB industry over 40 years as a designer, owner of a service bureau, and has also worked in marketing and engineering management at Racal-Redac, ASI, Cadence, PADS, and VeriBest. To contact him, [click here](#).

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## News Highlights



### **Miraco Earns ITAR Registration**

Miraco Inc. recently received an ITAR registration from the U.S. Department of State, Directorate of Defense Trade Controls (DDTC). Registration is a primary means to providing the U.S. Government with necessary information on who is involved in certain manufacturing, exporting, and brokering activities.

### **Survey Reveals Cost of Conflict Minerals Compliance**

The first year of conflict minerals reporting has come and gone, but how much did it cost? What lessons have we learned? A comprehensive Tulane University survey of 2013 issuers shows average costs per issuer, identifies qualitative measures issuers are currently using, and identifies common supply chain practices.

### **DSG Honored with Supplier Award from Honeywell Aerospace**

Dongguan Somacis Graphic (DSG) has received the 2014 Supplier of the Year Award for service and delivery performance at the 2014 Honeywell Aerospace Supplier Summit. "We are honored to receive this award in recognition of our service and delivery performance, but also as a testimony to the strong partnership we have enjoyed with Honeywell over the years," commented Giovanni Tridenti, CEO of DSG.

### **Invotec Receives BAE Systems Supplier Award**

This achievement is a reflection of Invotec's close working relationship with BAE Systems, the UK's largest manufacturer and provider of complex military equipment and technology and a founding member of the Aerospace Defence Security (ADS) 21st Century Supply Chain (SC21) program.

### **NPI Applauds Federal Competition to Create IP-IMI**

The National Photonics Initiative (NPI), an alliance of top scientific societies uniting industry and academia to raise awareness of photonics, applauded the Funding Opportunity Announcement (FOA) issued by the DOD, through the Air Force Research Laboratory, calling for concept papers for the establishment of an Integrated

Photonics Institute for Manufacturing Innovation (IP-IMI).

### **Teledyne Broadens Portfolio with Oceanscience Acquisition**

"Through the acquisition of Oceanscience, as well as the recent investment in Ocean Aero and the pending acquisition of Bolt Technology and its Sea-botix division, we will have significantly broadened Teledyne's portfolio of remotely-operated and autonomous marine systems," said Robert Mehrabian, chairman, president, and CEO of Teledyne.

### **Aerospace Suppliers Ramp Up to Meet Surging Orders**

The aerospace supply industry is still in the early days of a long-term boom in orders say industry participants at a recent suppliers' summit hosted by GE Capital at GE Aviation's headquarters in Cincinnati, Ohio. "We are in the midst of a 'super-cycle' of aerospace manufacturing," said Gib Bosworth, managing director of aerospace financing at GE Capital, Corporate Finance.

### **North America, APAC: Largest Military Radar Markets**

The global military radar market is expected to experience a CAGR of 1.05% during 2014–2024; North America and Asia-Pacific are expected to be the largest military radar markets, with a cumulative market share of more than 72%.

### **Global BYOD Security Market to See 35.23% CAGR**

Enterprise mobility and flexibility in operations are essential for organizational success, leading many large enterprises to encourage employees to access enterprise data from their personal devices. However, this introduces many security concerns.

### **Cybersecurity Spending to Reach \$109 Billion by 2020**

ABI Research calculates cybersecurity spending for critical infrastructure protection will reach US \$109 billion globally by 2020. The majority of spending will focus on securing the financial sector and the ICT infrastructure, with the North American and European regions pumping the most into network, systems, and data security.





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# Making a Connection with Conductor Discontinuities

by **John Coonrod**  
ROGERS CORPORATION

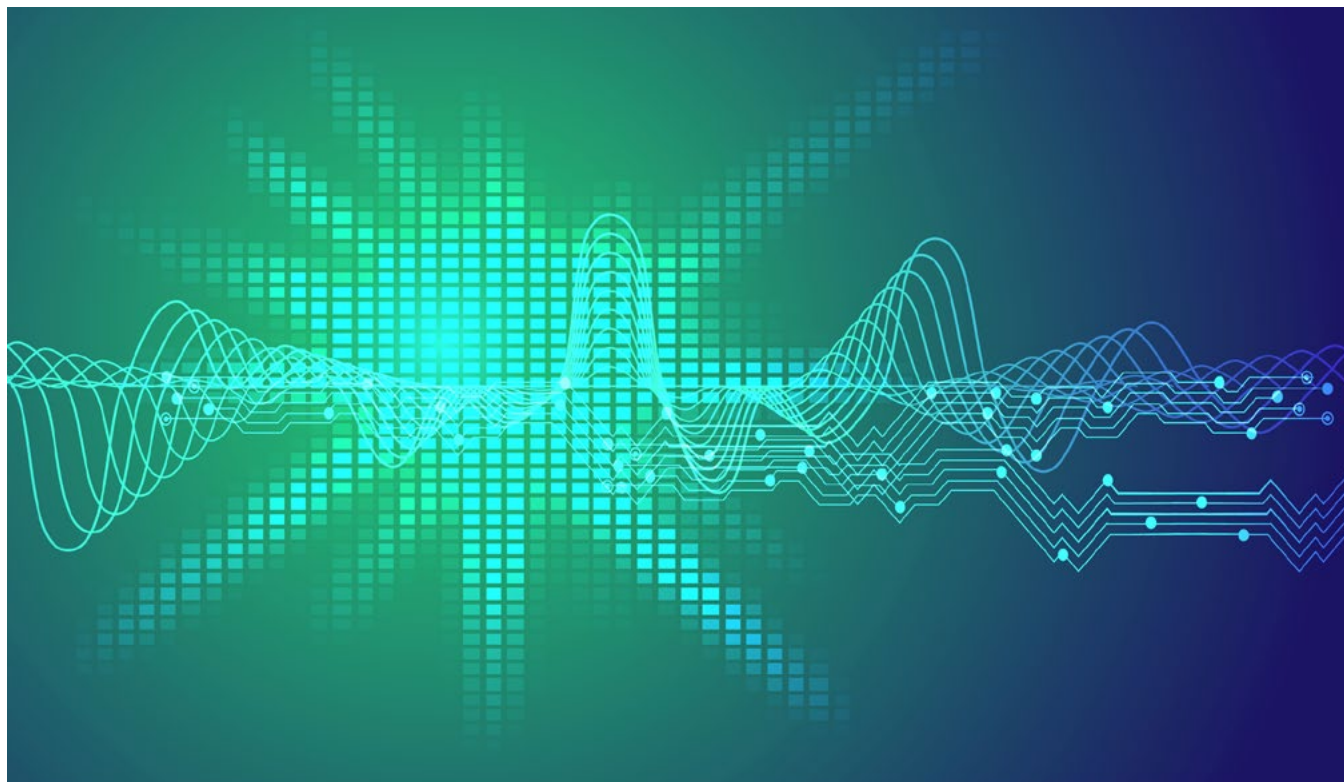
The title may be confusing for many technologists accustomed to dealing with electrical issues in traditional PCBs, but if you design PCBs that operate at microwave frequencies, it makes perfect sense. With microwave PCB design, it is not uncommon to have a conductor run come to a stop, followed by a space, followed by another conductor run, with the RF energy propagating through the discontinuity without the slightest problem. .

## Not Your Traditional Design

In traditional PCB design world, this conductor-space-conductor configuration is called an “open,” and it is considered a reject that yields a dead circuit. But microwave PCB design is much different. How does RF energy propa-

gate through conductor discontinuities in microwave PCBs?

When considering microwave technology, it is all about waves. Specifically, it is the electromagnetic (EM) wave that propagates on the PCB, and the wave properties are manipulated by the PCB design to get the desired circuit performance. To picture a simple example of an EM plane wave on a PCB, you can think of the wave in a cross-sectional view that looks like a sine wave. This sine wave will have different locations with high and low energy and  $\frac{1}{4}$  of the sine wave is one of the maximum power points. A  $\frac{1}{2}$  sine wave is where the wave returns to zero and has no energy. These fractions of the sine wave are appropriately called  $\frac{1}{4}$  wavelength and  $\frac{1}{2}$  wavelength, respectively.





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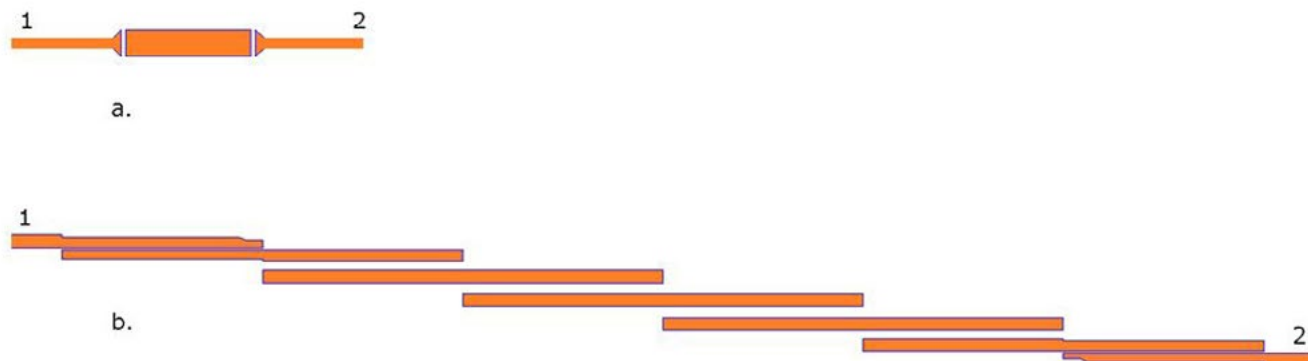
**MAKING A CONNECTION WITH CONDUCTOR DISCONTINUITIES** *continues*

Figure 1: Shown is the signal layer of a microstrip (a) gap coupled resonator and (b) edge coupled bandpass filter.

At microwave frequencies, a resonator can be made by using a conductor with a physical length that is exactly  $\frac{1}{2}$  wavelength of the wave on the circuit. This  $\frac{1}{2}$  wavelength conductor will resonate, which is accomplished by a wave that bounces back and forth and sets up a standing wave. The standing wave generates a lot of energy and resonates at the frequency associated with that  $\frac{1}{2}$  wavelength.

The big question is this: How do you get the energy on the conductor that is acting like a  $\frac{1}{2}$  wavelength resonator? If you have a conductor that connects to the  $\frac{1}{2}$  wavelength resonator, that combination creates a much longer conductor, and it no longer works as a  $\frac{1}{2}$  wavelength resonator. This means that you cannot directly connect to the resonator conductor and you will need to “couple” energy to the resonator. This is done by using feed line conductors on both sides of the  $\frac{1}{2}$  wavelength conductor, which are physically very close to the resonator conductor; as a result, the energy on the feed lines will have electric fields that radiate onto the resonator.

The radiated fields will couple electric energy onto the resonator, and now the conductor that is  $\frac{1}{2}$  wavelength long will resonate. An example of a  $\frac{1}{2}$  wavelength resonator, with feed lines on both sides of it, is shown in Figure 1a.

### Filtering Frequencies

Let's take this idea and expand it to make a filter. This filter example will only let energy pass from a band (range) of frequencies, and is

known as a bandpass filter. Due to the nature of the resonator, it is very frequency-dependent; in other words, the resonator will have a lot of energy only at a narrow range of frequencies. The tight range of frequencies for resonance is based on the physical length of the conductor being a  $\frac{1}{2}$  wavelength.

To illustrate, if higher frequencies are considered, the wavelength of that energy is shorter and the physical length of the resonator conductor is not correct for those frequencies that will not allow resonance. However, if you put together (couple) several resonators that are slightly different, they will resonate within a band of frequencies and let energy through within that range of frequencies. The resonators will not resonate outside of the frequencies of which they are the correct size, so the energy from those frequencies will be shut off. The resonators in our filter example will be put side-by-side so they can couple energy better from one resonator to the other, as shown in Figure 1b.

The best way to view the electrical performance of the bandpass filter is to show how much energy is passed through the filter and how much is rejected by the filter, when considering a wide range of frequencies. One method of doing this is by using a network analyzer and showing the S21 curve over a range of frequencies. The S21 parameter is a scattering (S) parameter, which basically shows how much of the energy that arrives at port 2 came out of port 1. It can be thought of as input and output for port 1 and 2 respectively, as shown in Figures 1a and



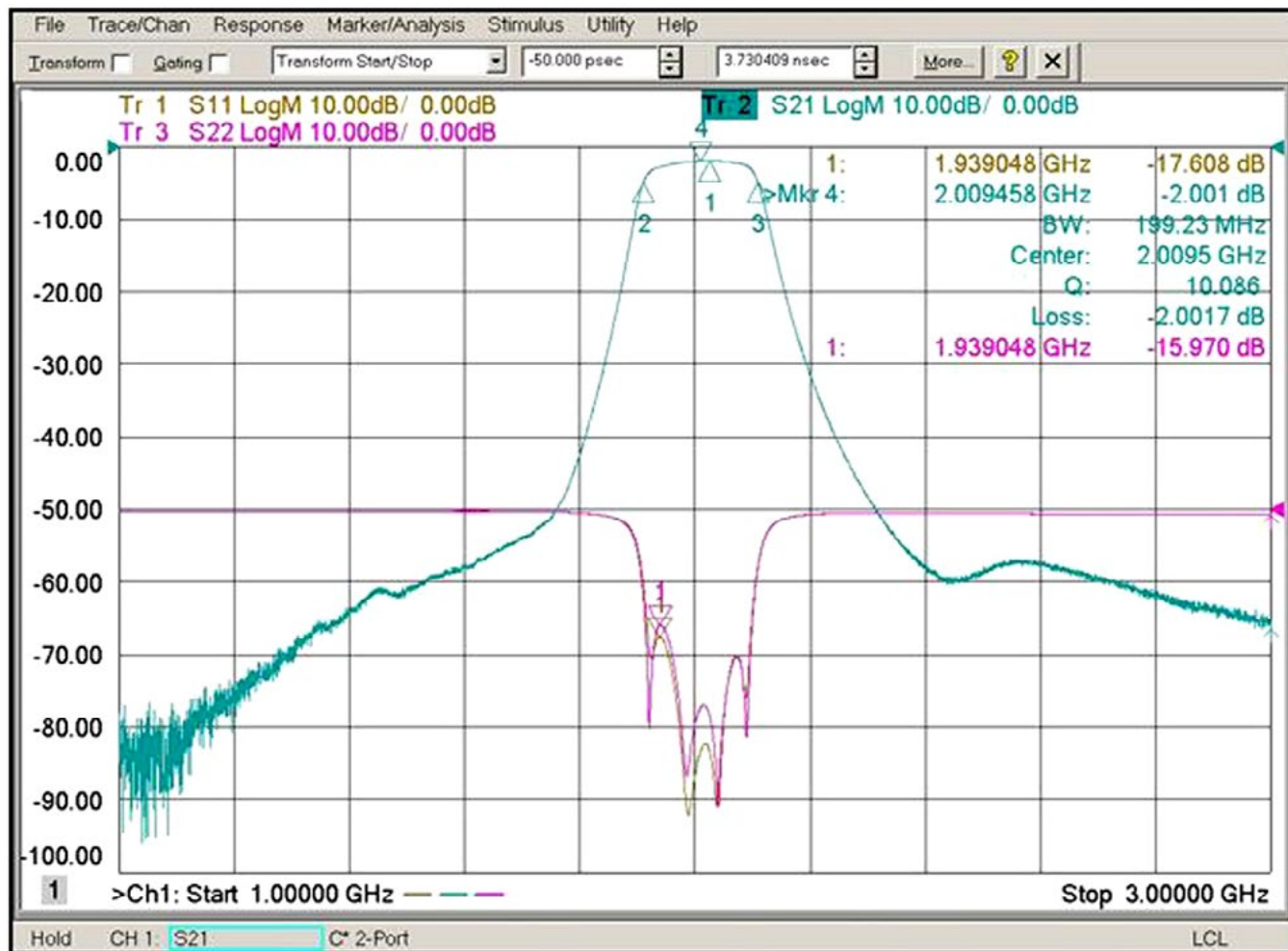


Figure 2: Frequency vs. S21 performance of a microstrip edge-coupled bandpass filter.

1b. A frequency-S21 curve for a microstrip edge-coupled bandpass filter is shown in Figure 2.

Even though there are multiple conductor discontinuities for the filter shown in Figure 1b, it can be seen that energy still propagates through this structure, given the energy is at the right frequency. In the case of the edge-coupled filter performance shown in Figure 2, a good example would have energy propagate through the filter at 2 GHz. The blue curve in Figure 2 shows S21 performance, and there is a band of frequencies, from about 1.9 to 2.1 GHz, at which much of the energy is passed through the filter. If an application was generating a lot of energy at 3 GHz (the far right frequency in Figure 2), the energy at that frequency is pretty much shut off with about 65 dB of loss.

## Summary

Contrary to many of the concepts related to traditional PCBs, conductor discontinuities at microwave frequencies may not cause a defect in a circuit, and they could actually be the reason the circuit is performing properly. Additionally, there are many other design issues to consider when designing microwave PCB circuitry, and the rules regarding typical PCBs no longer apply. **PCBDESIGN**



John Coonrod is a market development engineer for Rogers Corporation, Advanced Circuit Materials Division. To read past columns, or to reach Coonrod, [click here](#).

# Like it or Not, You're a Role Model

by Tim Haag

INTERCEPT TECHNOLOGY

Except for the rather obvious similarity to a vegetable, the name Albert Romolo Broccoli may not ring any bells for you. But if I were to mention his nickname "Cubby," you might remember this man as the American film producer who originated the James Bond movie series.

One day, while still a boy in New York, Cubby noticed an airplane flying overhead. It was the Spirit of St. Louis, flown by none other than Charles Lindbergh. Cubby waved excitedly to the plane and to his delight, Lindbergh returned his wave. Later, Cubby would say that this moment made him realize that in America anyone can achieve anything if he puts his mind to it.

We could talk at length about how Cubby took this moment and used it to motivate his

life. We could discuss how he overcame great obstacles and navigated massive disappointments, including early failed movie projects and the death of his second wife, only to later build a film dynasty around a simple series of three digits, 007. It is an inspirational story of perseverance and accomplishment. But let's look at this story from a different perspective instead.

I would imagine that Charles Lindbergh had no idea that day, as he waved back at people on the ground below, that one of them was a future movie producer. The thought that his casual salutation could motivate someone to achieve greatness probably never crossed his mind. I bet that he waved to hundreds, if not thousands, of people as he flew over them. The point is, he



Figure 1: Charles Lindbergh, famed aviator and role model for many.



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## LIKE IT OR NOT, YOU'RE A ROLE MODEL *continues*

could have chosen NOT to wave to anyone. He was, after all, a world record-setting pilot and he had important things to do and to concentrate on, not the least of which was flying an airplane.

The Spirit of St. Louis was not the easiest plane to fly; designed for distance, it featured a large fuel tank between the pilot and the engine, completely blocking Lindbergh's forward view. He had to swing the plane from side to side to look out the side windows, or peer through a small periscope in order to see what was in front of him. I don't think that any of us could blame him if he had chosen to focus his attention to the difficult task of flying instead of waving to people.

And yet he did choose to wave on that day without realizing what that simple act could accomplish. He was a role model, whether he knew it or not.

When I was in high school, I worked at a mom and pop hamburger restaurant, for a man named John. Even though he could be gruff at times, John would let us do our homework when the restaurant was slow and made sure that we always had something to eat. John set a terrific example by being there every day, working steadily, and showing an interest in the life and well-being of all the teenagers who worked for him. His management and care for us helped shape my own character as I grew.

Likewise, during the years that I built my skills as a circuit board designer, many people helped shape my character. Some were impulsively brilliant at laying out a board, while others were steady and consistent in their approach to work, dotting every "i" and crossing every "t." But they were all patient with me, answering my questions, showing me the ropes, and setting good examples for me to follow.

So today when I am confronted with a problem or situation that is difficult to get through, I often reflect on what I learned from these mentors. Their examples have helped me numerous times to work through a tough situation that requires either wise management or intricate technical skills. I am very fortunate to have all of these different examples to fall back on. These mentors became my role models.

We will never know how much our actions

affect other people, but the fact is that people are impacted all the time by what we do and say. For instance, consider the story of George Bailey in the movie "It's a Wonderful Life." George lived his life working himself to death for some hoped-for future momentous event, all the while missing the minor miracles that happened around him every day. He refused to recognize how his contributions had a positive impact in the life of others until the latter part of the movie when he is forced to see what life without him would be like. Not only were the people that he knew and loved in bad shape due to his absence, but his entire town was radically different for the worse. And it was all because he hadn't been there as a positive influence.

Now true, that was just a movie. But contrast that make-believe story with the real-life example of Charles Barkley. He sparked public outrage several years ago when he said, "I am not a role model." Here's the key: We are all role models. We just have to decide if we are going to be a good role model or a bad one.

I recently read a blog written by Air Force Col. Donald Grannan, 88<sup>th</sup> Communication Group Commander, describing how a young lady not in his command, a staff sergeant who was ascending rapidly in her Air Force career, abruptly resigned from the service. The reason for her departure? She felt that the Air Force had clearly demonstrated that it didn't want her. How could someone with such a bright future in front of her end up with this negative impression of the Air Force? It wasn't a matter of poor performance on her part or a lack of motivation. She had received top marks on all of her performance reports, taken part in two deployments, and was considered a "superstar" among her peers.

The colonel found instead that the problem lay with her leadership team. When she had a conflict with a senior co-worker (who was in the wrong), none of her leaders offered to intervene, counsel, or help in any way. When she was promoted to staff sergeant the first time she was eligible, it took days before anyone complimented her on this accomplishment, and was never recognized by her commander. When she became a distinguished graduate from Airman Leadership School, a highlight in her career, no



one from her squadron's chain of command was present except for her immediate supervisor. But because she had once failed a physical fitness test (and immediately re-took it and passed), this one mistake was the point in her career that was magnified.

The colonel wrote that her leadership had been gifted with an exceptional team member, but failed to mold her, encourage her, or create a new leader. The Air Force didn't bother to honor her on her way out the door. Instead, her leaders focused on her one small error, her failed fitness test, and the result was that the service lost a valuable member of the team.

Whether you wear a neatly pressed uniform with shiny medals, a suit and tie, a hard hat, or an apron, at the end of the day it's how you foster an environment of growth that will make the difference in how successful your business is for the long term. Are we being a positive role model to those who work for us and with us? Are we leading by example and helping others to grow? And then, are we extending this prin-

ciple beyond the realm of business, by investing ourselves in a similar fashion to those from the other areas of our lives? Setting a good example and being a positive influence could be the difference that will make our companies a success, our families tight, and our friendships rich.

So the next time we are in a situation where someone looks at us for help, leadership, or just a good example of how something should be done, remember that a simple wave once helped launch the career of a super spy that has saved the world many times over now. Who knows what a similar wave on our part might end up doing for the person who receives it?



Tim Haag is customer support and training manager for Intercept Technology.

## video interview

### SMTA President Highlights Technical Programs at SMTAI

*by Real Time with...*  
**SMTAI**



SMTA President Bill Barthel joins Editor Ray Rasmussen to discuss the outstanding technical programs and standards committees offered during SMTA International—part of the partnership between SMTA and IPC. Barthel also previews upcoming association learning and training events.



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# TOP TEN

PCBDesign007  
News

## News Highlights from PCBDesign007 this Month

### ① **Mentor Launches FloEFD Product with Enhanced Capabilities**

The company announces the latest release of its award-winning FloEFD upfront and concurrent computational fluid dynamics (CFD) product. This new release provides advanced capabilities and functionality which enables designers and analysts to create more realistic operating environments and models for improved simulation accuracy.

### ② **Intercept Releases Expanded EMSAT Viewer**

Intercept Technology Inc. announces the availability of a new and improved low-cost electromagnetic compatibility (EMC) solution. The software solution pairs the EMSAT post-layout EMC and SI design rule checkers, developed by IBM and sold through Moss Bay EDA, with a customized Pantheon EMSAT Viewer that displays each violation on the board in real-time.

### ③ **Zuken Seeks Presentation for Innovation World Americas**

Zuken is now accepting presentation proposals for the 2015 Zuken Innovation World Americas Conference taking place June 1-3, 2015 in San Diego, California. Topics focused on board design, electrical and harness design, design data management, and innovative technologies are welcome. Case studies, challenging design experiences, new technology trends or solutions to a common design problems are particularly sought.

### ④ **Institute of Circuit Technology's 2014 Darlington Seminar**

Editor Pete Starkey recently made a trip to the Northeast of England for the Institute of Circuit Technology's annual Darlington Seminar. Highlights included a presentation from Ventec's Martin Cotton on practical design considerations for high-speed PCBs—"Design once, make many times" was his main message—and a talk from Dr. Andrew Cobley addressing the rise of wearable technology.



## 5 Westdev Debuts Pulsonix 8.5 Design Software

Westdev Ltd. has released its latest professional PCB design software, Pulsonix 8.5. This release introduces new features which aid our customer-base in their transition of products to market and refinements with their everyday working systems.

## 6 Sanmina's India Design Center Earns ISO 13485

Sanmina Corporation announced that its India Design Center (IDC) has been awarded the ISO 13485:2003 and EN ISO 13485:2012 certifications for medical product design and development. Achieving these certifications recognizes the company's continuing expansion of its global medical design and manufacturing capabilities.

## 7 Cadence Professorship Endowed at Stanford

Cadence Design Systems, Inc. has announced the endowment of the Cadence Design Systems Professorship at Stanford University in the School of Engineering and the appointment of Dr. Kunle Olukotun as the first Cadence Professor. Dr. Olukotun is a Professor of Electrical Engineering and Computer Science and is the director of the Pervasive Parallelism Lab at Stanford University.

## 8 Harley Thermal Launches SolariaPCB Add-on to Solaria

Harley Thermal LLC has released the SolariaPCB add-on to Solaria, the company's powerful, low-cost general purpose thermal simulation software tool. SolariaPCB makes the tedious task of thermal modeling PCBs quick and easy. The ECAD interface brings in every trace, via, component, and layer. A component library of over 400 parts is included.

## 9 Ucamco Issues Latest Generation of Gerber X2

One of the new format's most powerful features is its board stack-up information capability. With X2, the precise function of each layer file, and its location within the stack-up, is clear and unequivocal, so stack-up data is generated automatically together with the image files. Drill and rout files, too, are fully automatically loaded and qualified, right from the start, thanks to the X2 format's wide-ranging functionality.

## 10 True MCAD and ECAD Integration

How many spins does it take to achieve proper electro-mechanical integration? The collaboration between the electronic and mechanical design domains are manual, reactive, inefficient, and outdated, but it doesn't have to be.

**PCBDesign007.com for the latest circuit design news—anywhere, anytime.**



# events

For the IPC Calendar of Events, [click here](#).

For the SMTA Calendar of Events, [click here](#).

For a complete listing, check out  
*The PCB Design Magazine's* [event calendar](#).



## **Front-End Design Summit 2014**

December 11, 2014  
San Jose, CA

## **CDNLive Silicon Valley 2015**

March 10-11, 2015  
Santa Clara, CA

## **DesignCon 2015**

January 27-30  
Santa Clara, California, USA

## **SMTA Pan Pacific 2015**

February 2-5, 2015  
Hawaii, USA

## **MEDIX 2015**

February 4-6, 2015  
Osaka, Japan

## **IPC APEX Expo 2015**

February 24-26, 2015  
San Diego, California, USA





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**Coming Soon to  
The PCB Design  
Magazine:**

**January:  
What's Ahead  
in 2015?**

**February:  
High-Speed  
Design**

**March:  
DFM**